



Chapter 1

INTERGRATED-CIRCUIT

LOGIC FAMILIES



Faculty of Computer Science and Engineering
Department of Computer Engineering

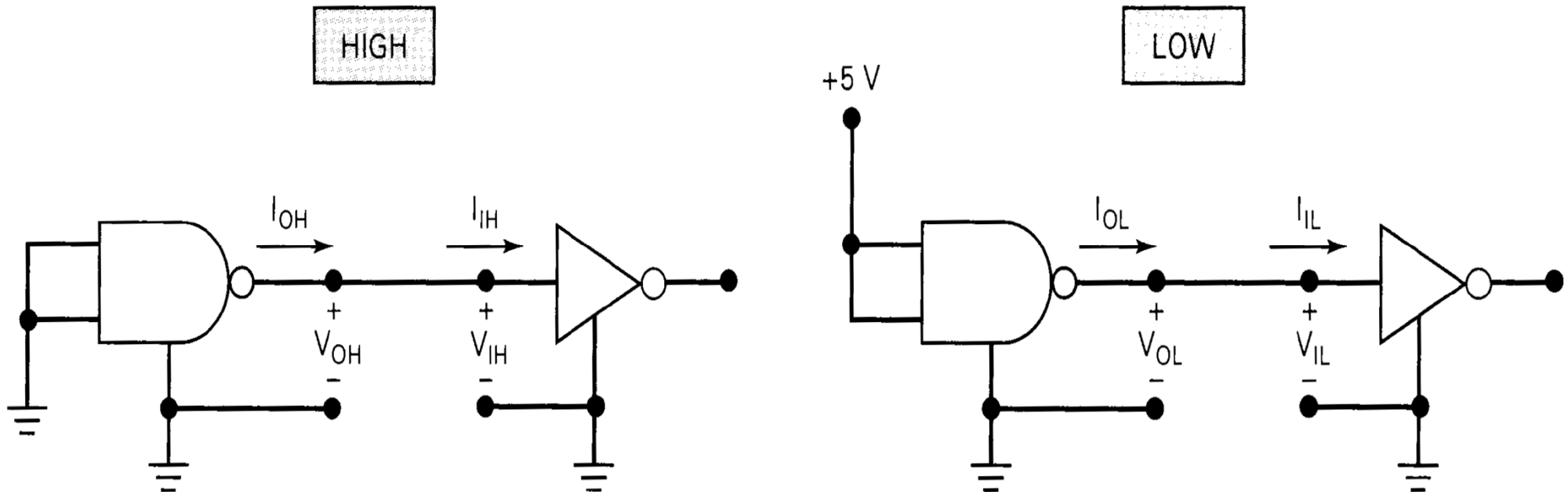
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Outline

- Digital IC Terminology
- TTL Logic Family
- MOS Technology
- Open-Collector/Open-Drain Outputs
- Tristate (Three-State) Logic Outputs
- IC Interfacing

Digital IC Terminology

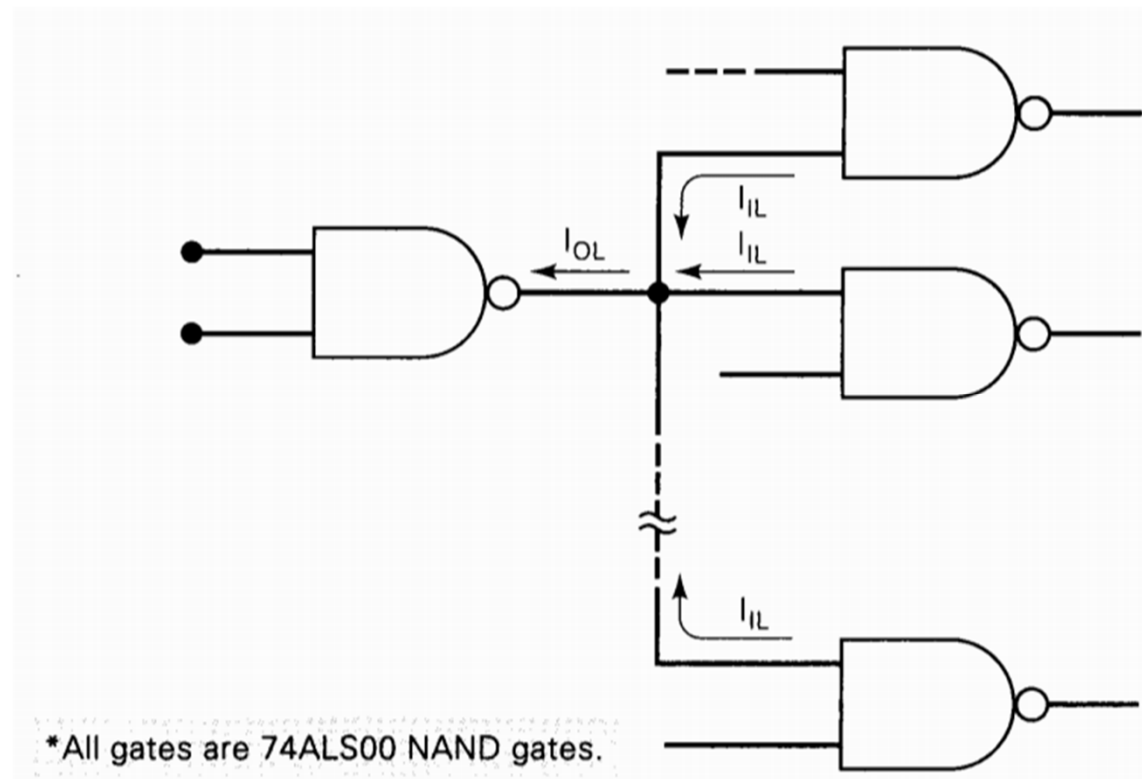


Current and Voltage Parameters

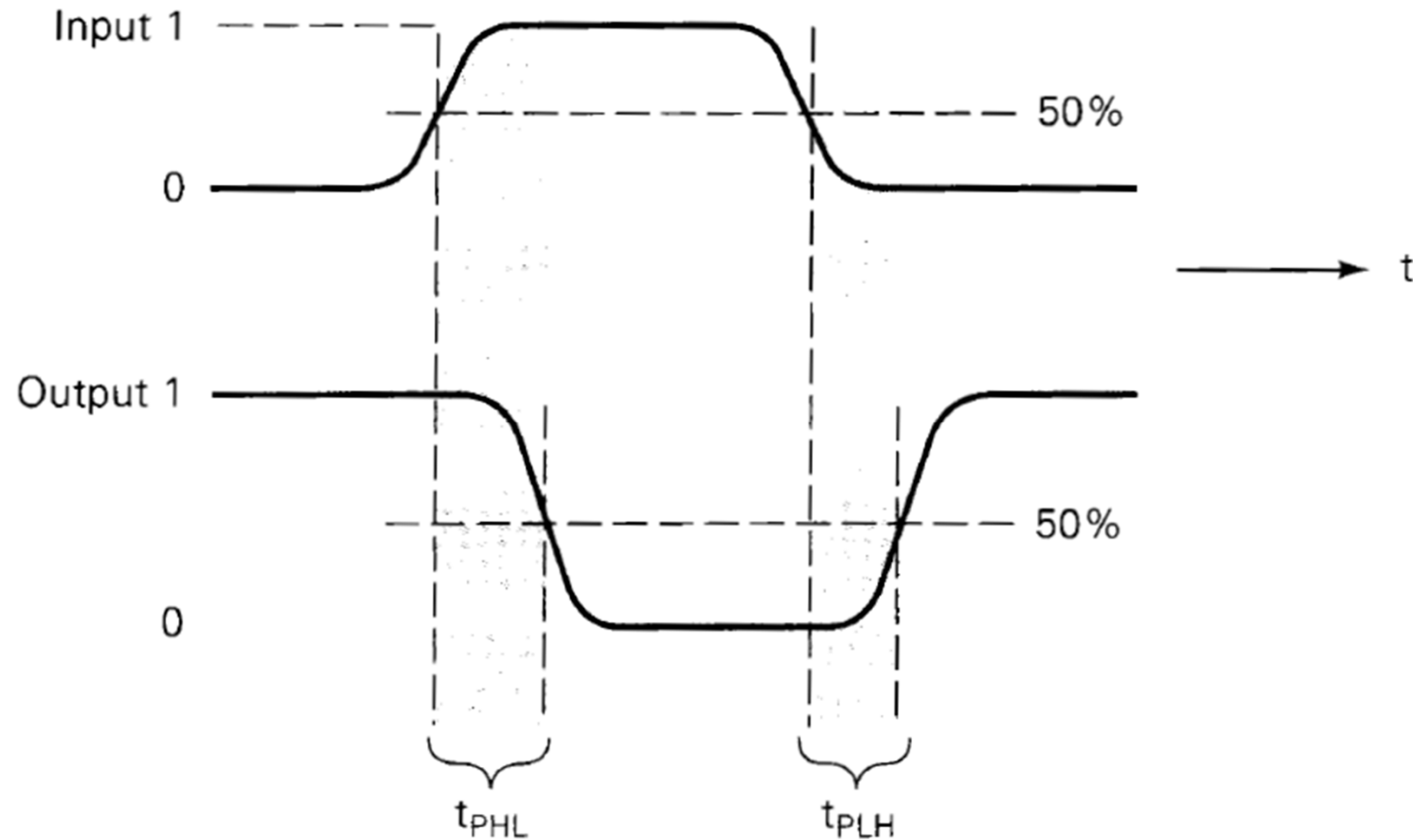
- ❑ **HIGH** logic:1 ; **LOW** logic :0
- ❑ $V_{IH}(\text{min})$ – High Level Input Voltage
- ❑ $V_{IL}(\text{max})$ – Low Level Input Voltage
- ❑ $V_{OH}(\text{min})$ – High Level Output Voltage
- ❑ $V_{OL}(\text{max})$ – Low Level Output Voltage
- ❑ I_{IH} – High Level Input Current
- ❑ I_{IL} – Low Level Input Current
- ❑ I_{OH} – High Level Output Current
- ❑ I_{OL} – Low Level Output Current

Fan-out

- Loading factor
- The maximum number of logic inputs that an output can drive reliably

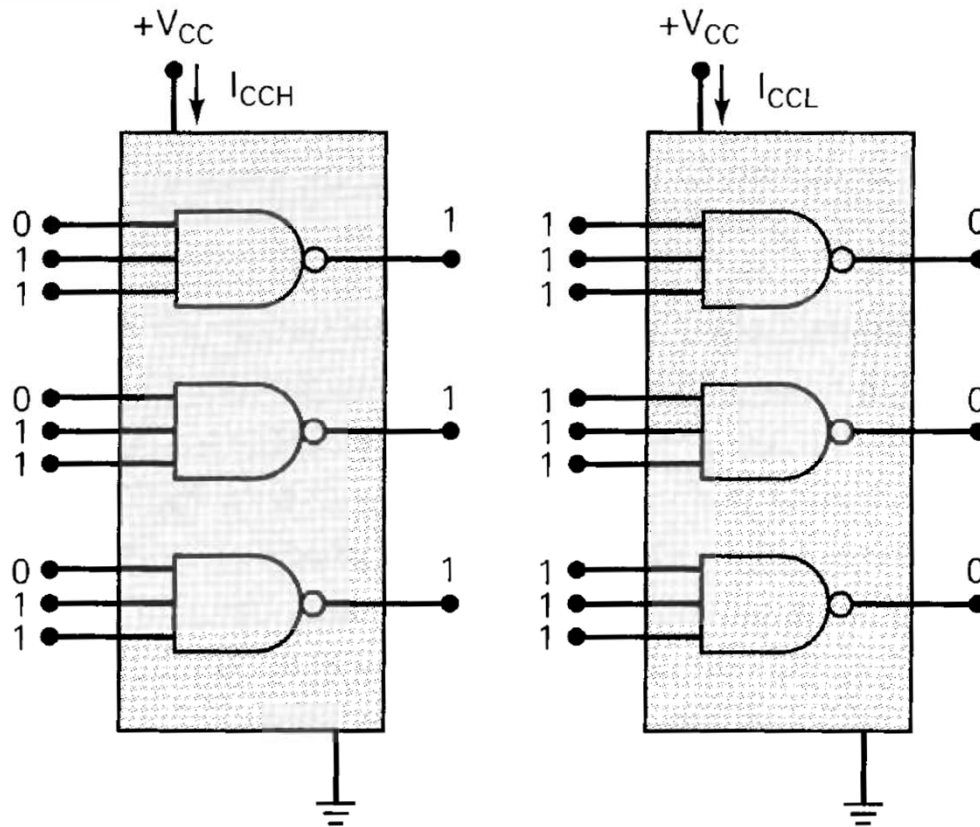


Propagation Delays



- ❑ t_{PLH} : Delay time in going from 0 \rightarrow 1 (LOW \rightarrow HIGH)
- ❑ t_{PHL} : Delay time in going from 1 \rightarrow 0 (HIGH \rightarrow LOW)

Power Requirement



- TTL devices: V_{CC}
- MOS devices: V_{DD}
- I_{CCH} : all outputs are HIGH
- I_{CCL} : all outputs are LOW

$$I_{CC(avg)} = \frac{(I_{CCH} + I_{CCL})}{2}$$

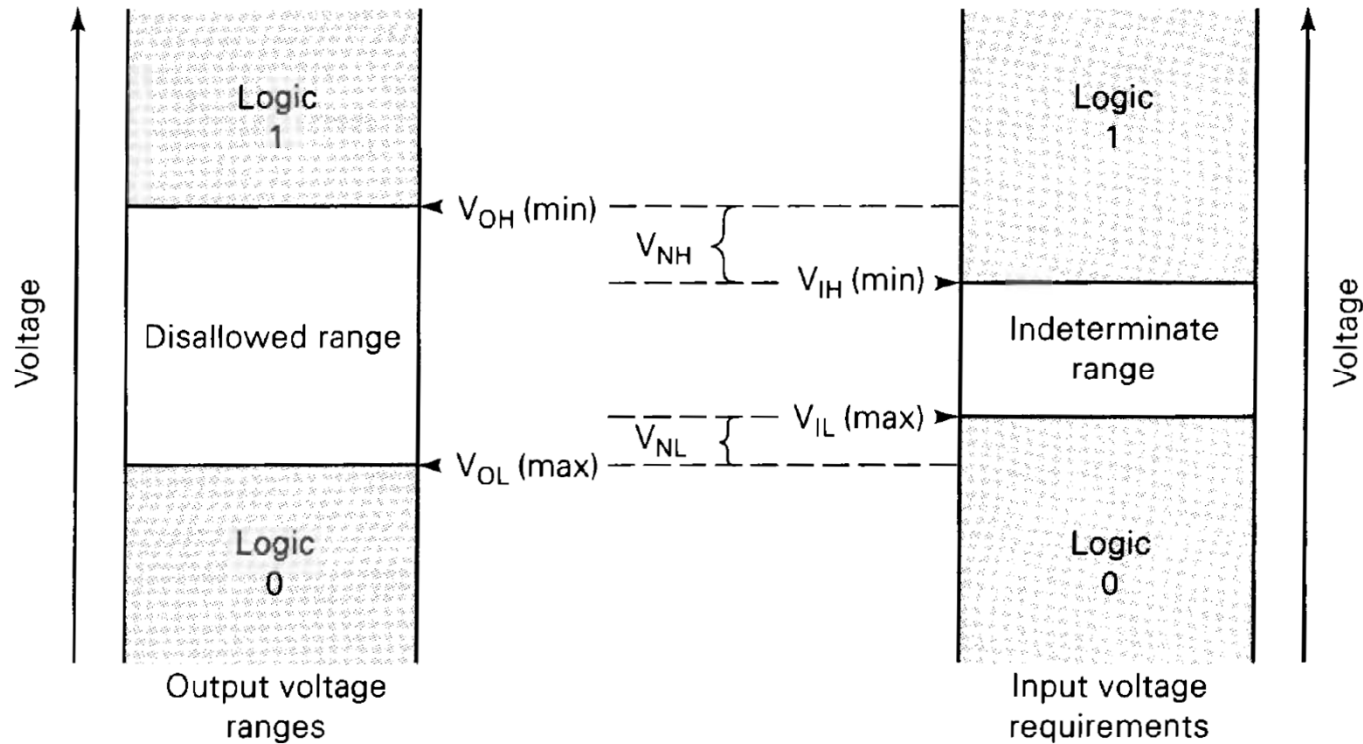
$$P_{D(avg)} = I_{CC(avg)} \times V_{CC}$$

Speed-Power Product

- Digital IC families desire:
 - Higher speed (shorter gate propagation delay) : S
 - Maximum average propagation delay
 - Lower power dissipation: P
 - Measuring and comparing the overall performance of an IC.

$$\text{Speed-power product} = S * P$$

Noise Immunity



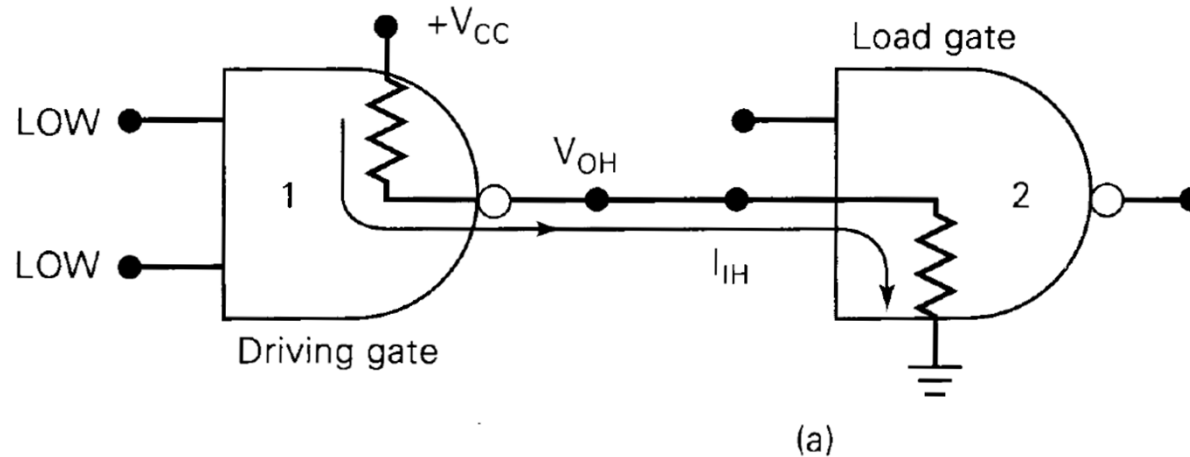
- *high-state noise margin*

$$V_{NH} = V_{OH}(\text{min}) - V_{IH}(\text{min})$$

- *low-state noise margin*

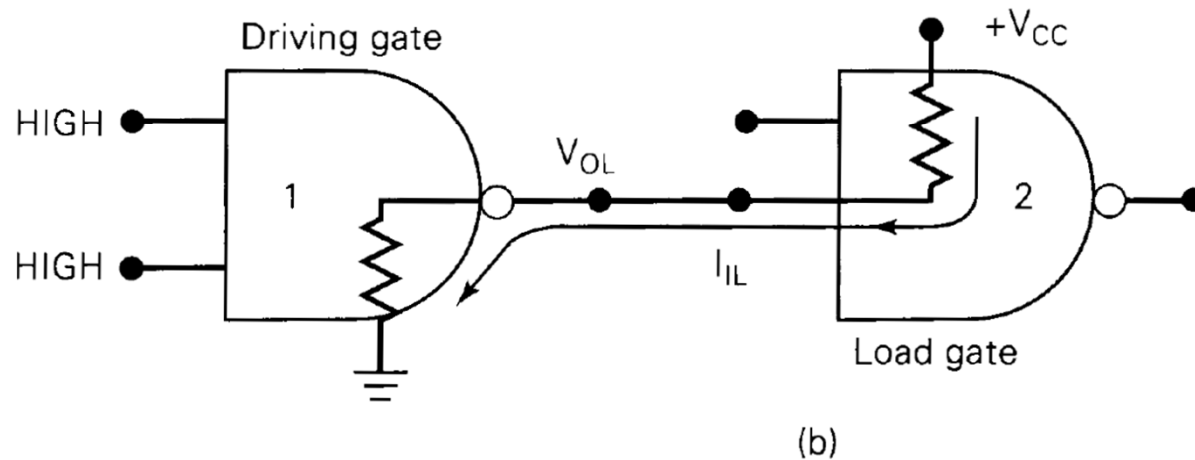
$$V_{NL} = V_{IL}(\text{max}) - V_{OL}(\text{max})$$

Current-Sourcing – Current-Sinking Logic



Current sourcing

Driving gate supplies (sources) current to load gate in HIGH state.

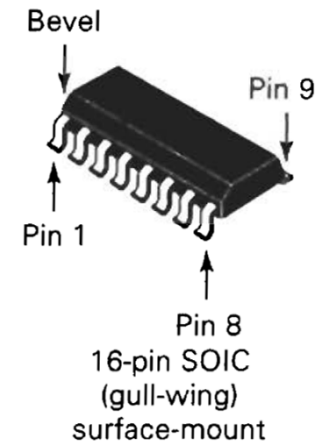
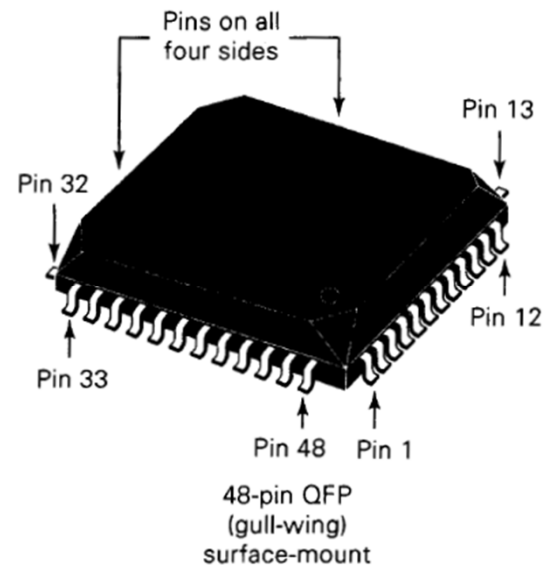
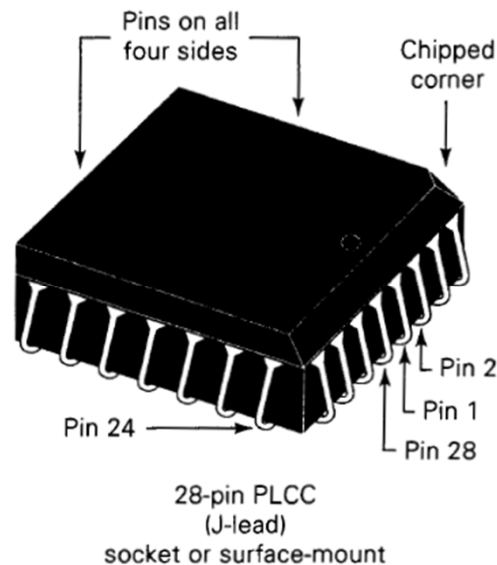
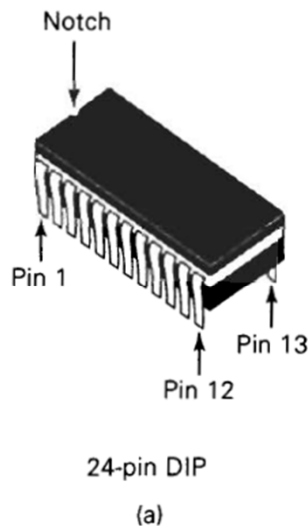


Current sinking

Driving gate receives (sinks) current from load gate in LOW state.

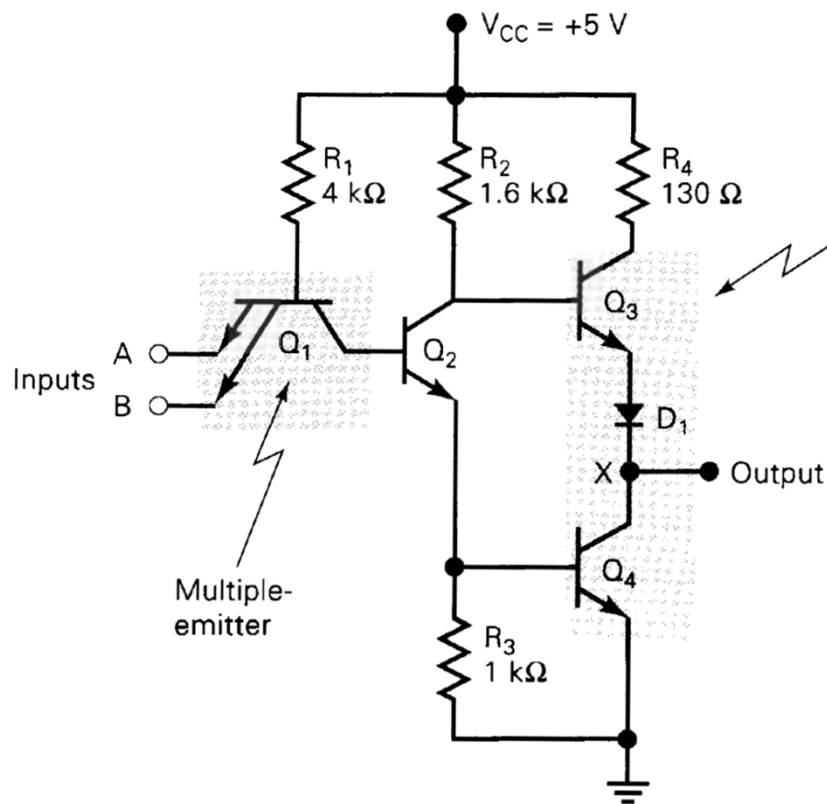
IC Packages

- DIP (dual-in-line package)
 - Lead pitch: spacing between pins (100 mils)
- Surface-mount

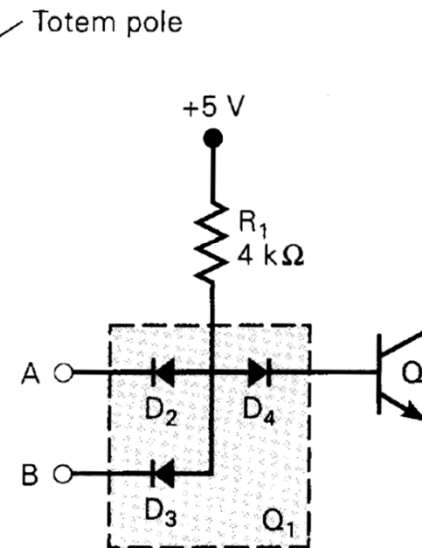


TTL Logic Family

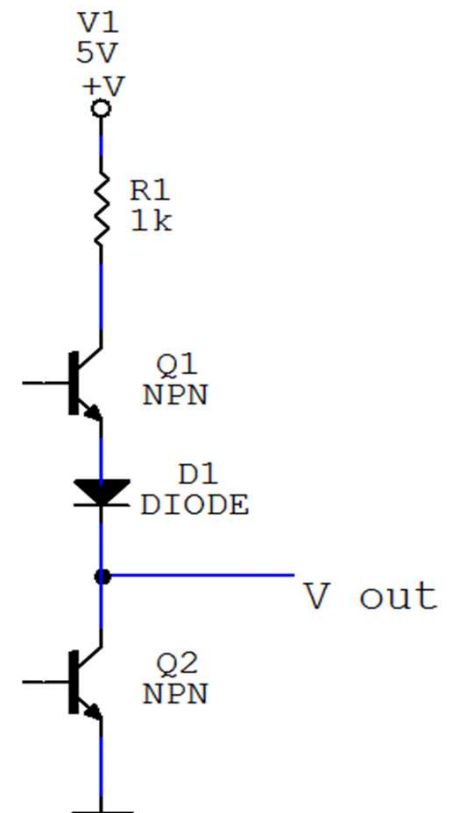
- TTL inputs: *multiple-emitter*
- TTL outputs: *totem-pole*



(a)

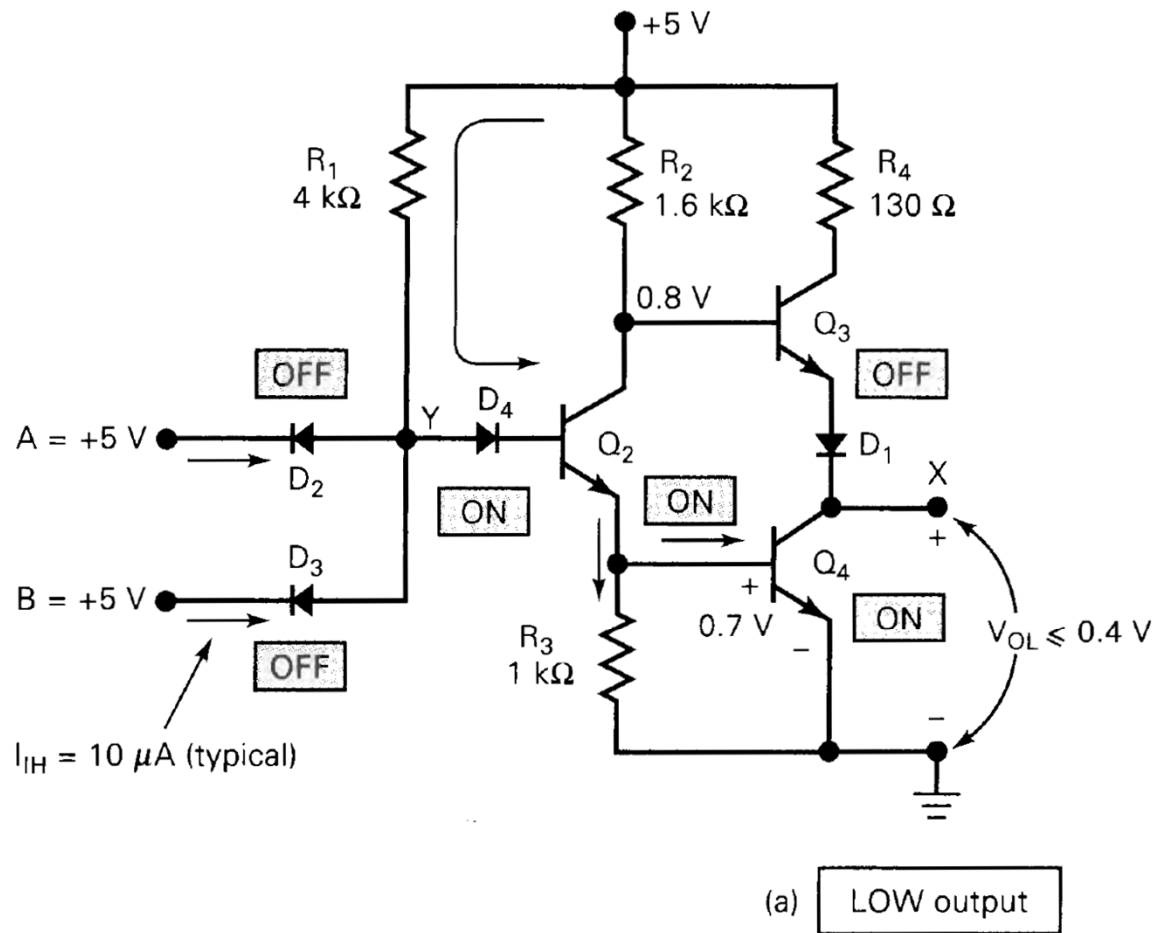


(b)



TTL NAND Gate

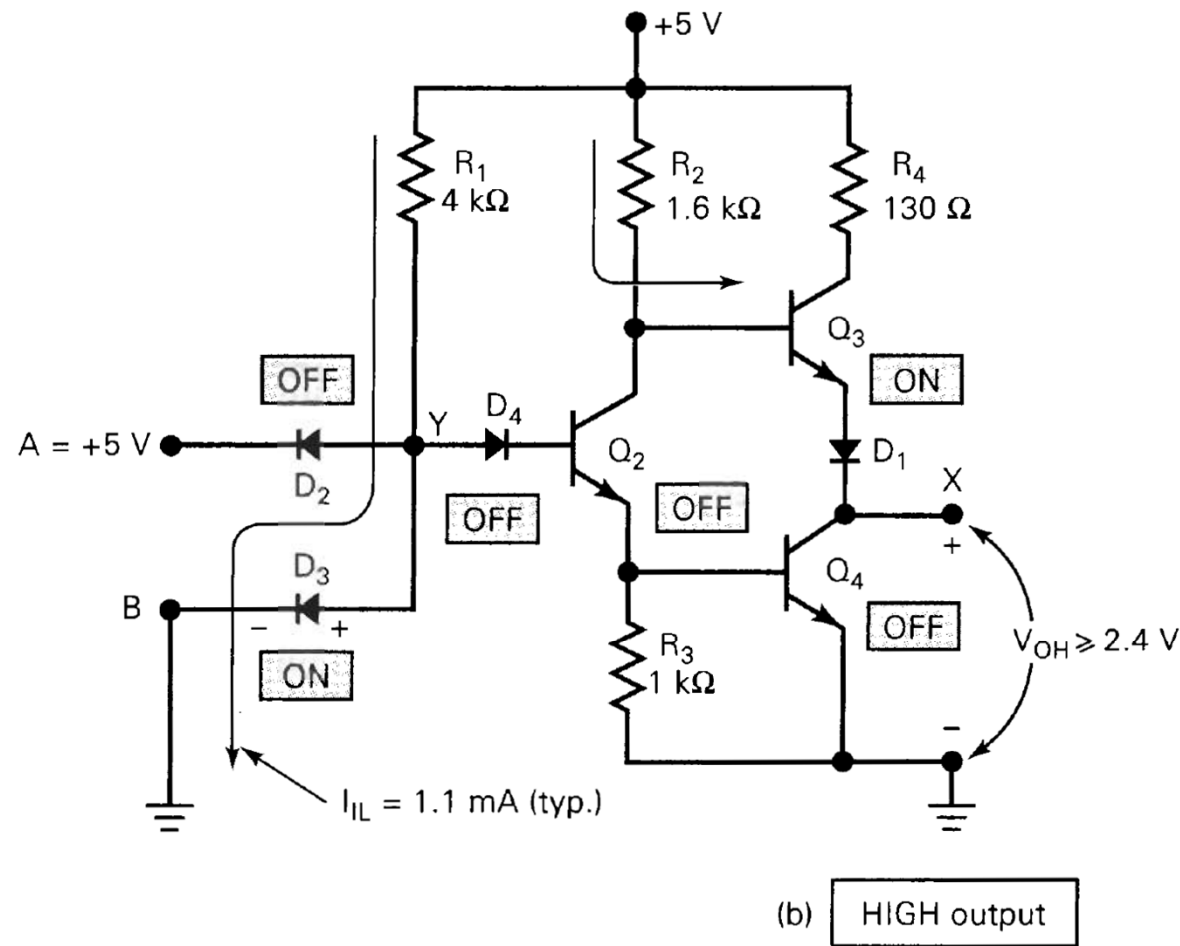
- LOW State



Input conditions	Output conditions
A and B are both HIGH (≥ 2 V)	Q_3 OFF
Input currents are very low $I_{IH} = 10$ μ A	Q_4 ON so that V_X is LOW (≤ 0.4 V)

TTL NAND Gate

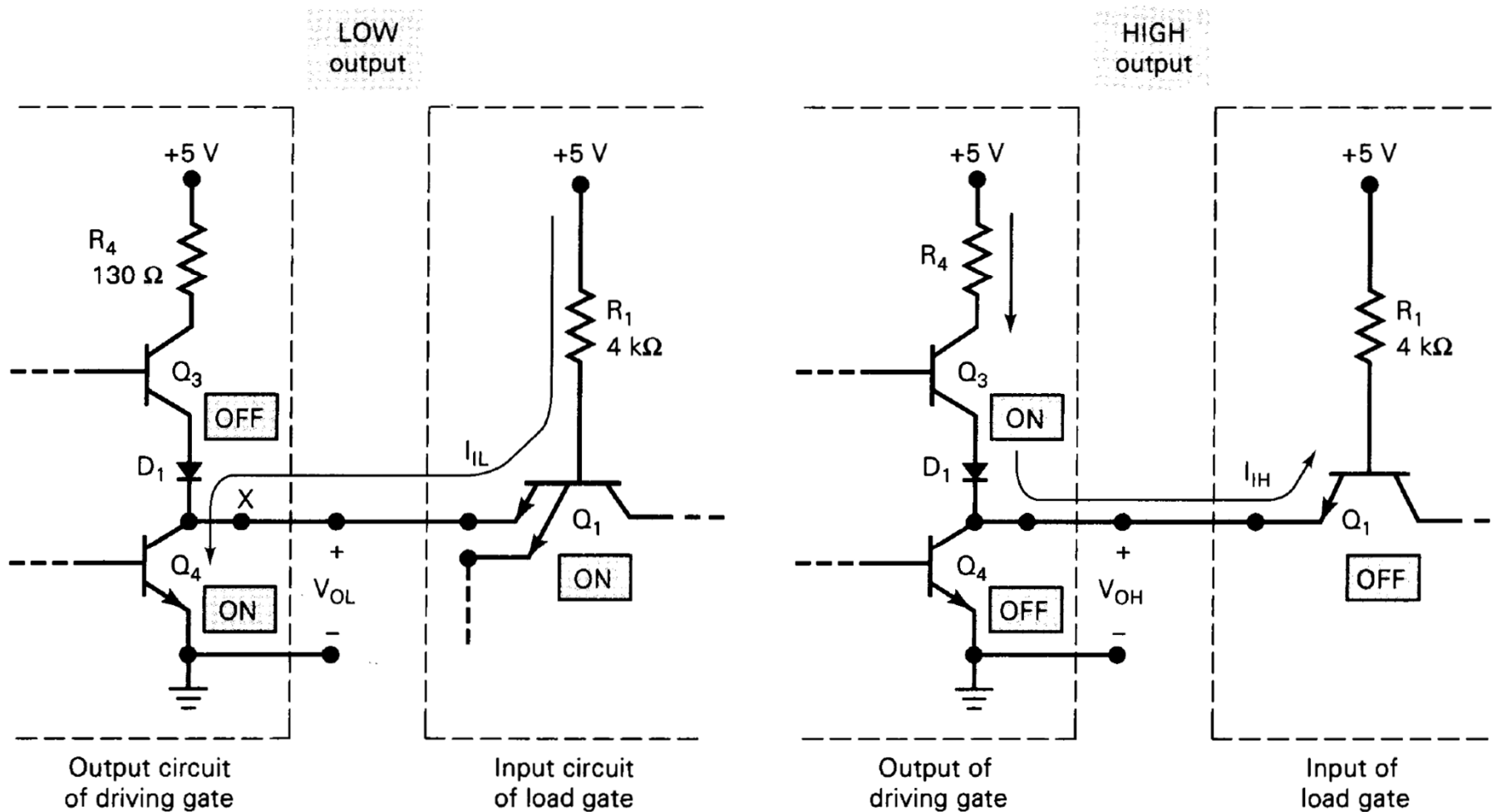
- HIGH State



Input conditions	Output conditions
A or B or both are LOW (≤ 0.8 V)	Q_4 OFF
Current flows back to ground through LOW input terminal $I_{IL} = 1.1$ mA	Q_3 acts as emitter-follower and $V_{OH} \geq 2.4$ V, typically 3.6 V

TTL NAND Gate

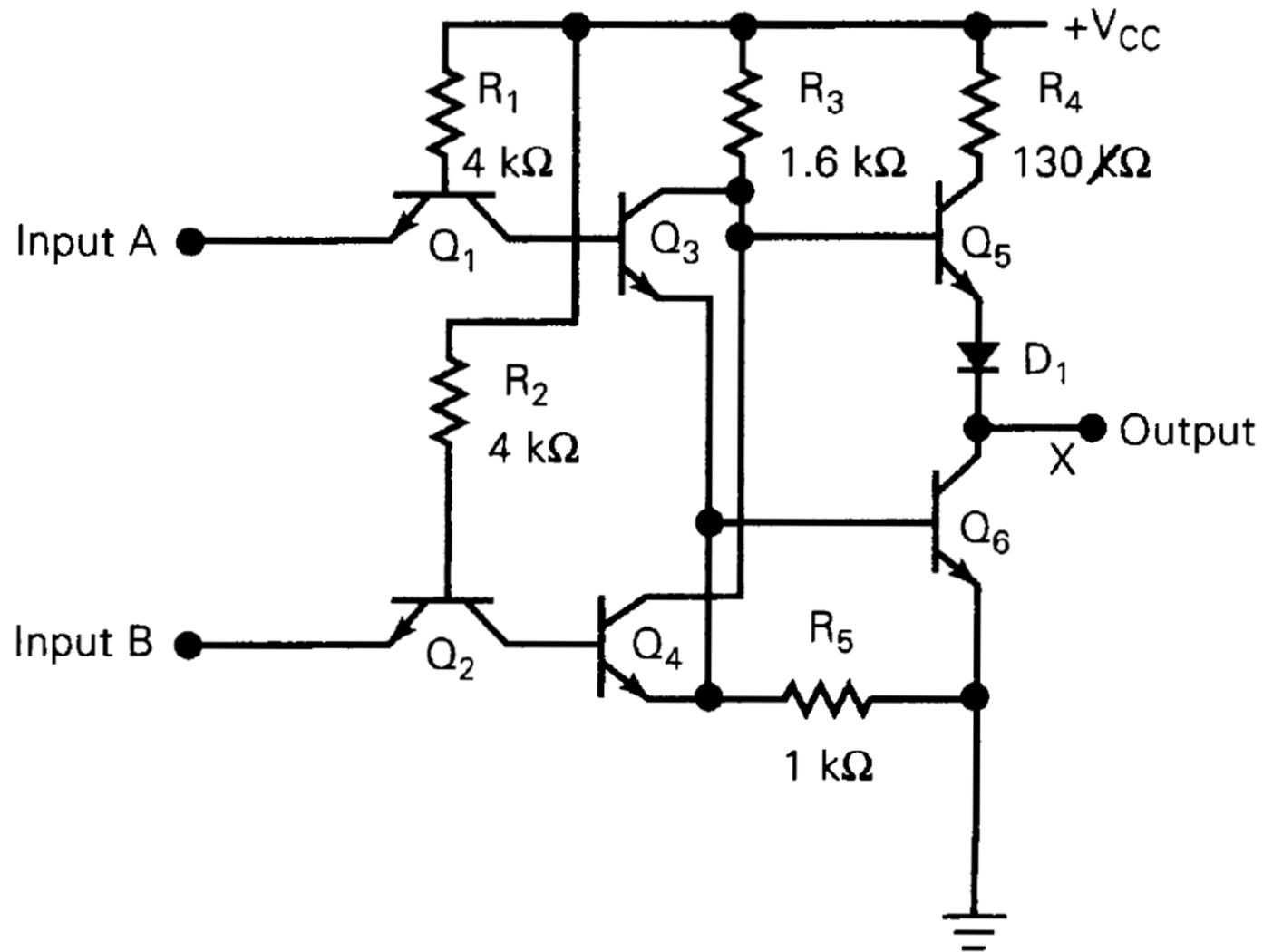
- Current-Sinking and Current Sourcing



TTL NAND Gate

- Totem-Pole Output
 - Advantage
 - Low power dissipation
 - Fast rise-time
 - Disadvantage
 - Large current spike during switching from LOW to HIGH

TTL NOR Gate



TTL Series

- Standard TTL, 74
- Schottky TTL, 74S
- Low-Power Schottky TTL, 74LS (LS-TTL)
- Advanced Schottky TTL, 74AS (AS-TTL)
- Advanced Low-Power Schottky TTL, 74ALS
- 74F-Fast TTL

TTL Data Sheets

- Supply Voltage – Temperature Range
- Voltage Levels
 - $V_{IL}, V_{OL}, V_{OH}, V_{IH} \rightarrow V_{NL}, V_{NH}$
- Maximum Voltage Ratings
- Power Dissipation
 - $I_{CCH}, I_{CCL} \rightarrow I_{CC}(avg) \rightarrow P_D(avg)$
- Propagation Delays
 - $t_{PLH}, t_{PHL} \rightarrow t_{pd}(avg)$

TTL Data Sheets

PARAMETER	TEST CONDITIONS		SN54ALS00A			SN74ALS00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$				-1.2			-1.5	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$				0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$				20			20	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$				-0.1			-0.1	mA
$I_{O\ddagger}$	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$		-20		-112	-30		-112	mA
I_{CCH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0$			0.5	0.85		0.5	0.85	mA
I_{CCL}	$V_{CC} = 5.5 \text{ V}$, $V_I = 4.5 \text{ V}$			1.5	3		1.5	3	mA

TTL Data Sheets

		SN54ALS00A			SN74ALS00A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8 [‡]			0.8	V
				0.7 [§]				
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54ALS00A		SN74ALS00A		
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	3	15	3	11	ns
t _{PHL}			2	9	2	8	

TTL Data Sheets

- Loading and Fan-out

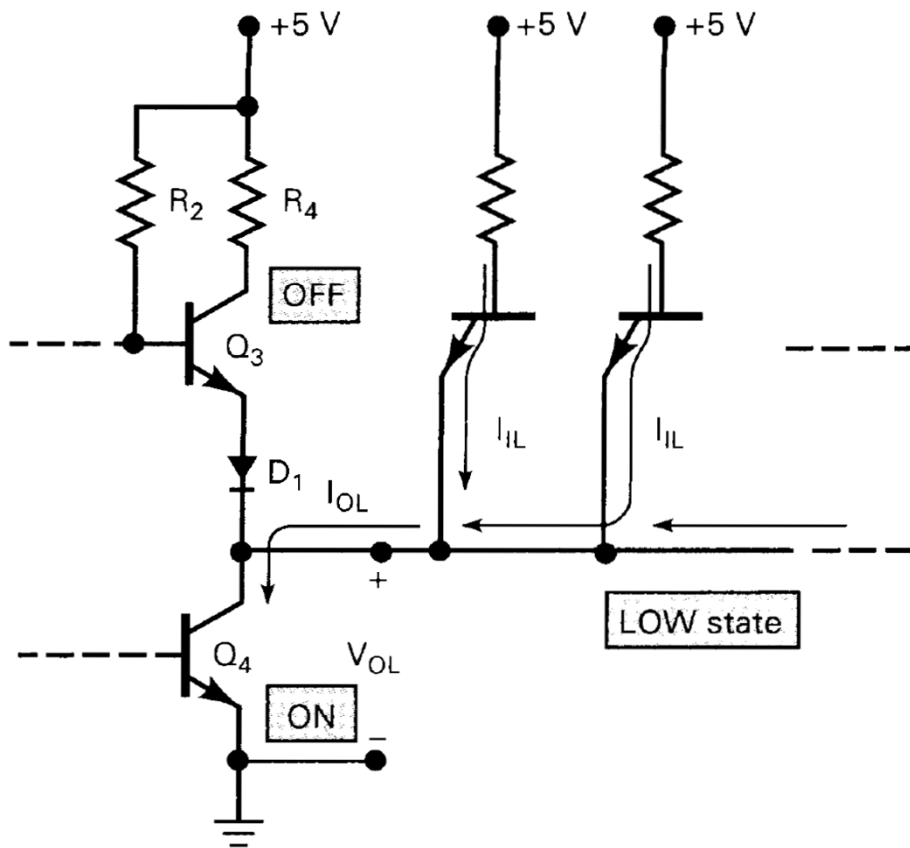
$$\text{fan-out(LOW)} = \frac{I_{OL}(\text{max})}{I_{IL}(\text{max})}$$

$$\text{fan-out(HIGH)} = \frac{I_{OH}(\text{max})}{I_{IH}(\text{max})}$$

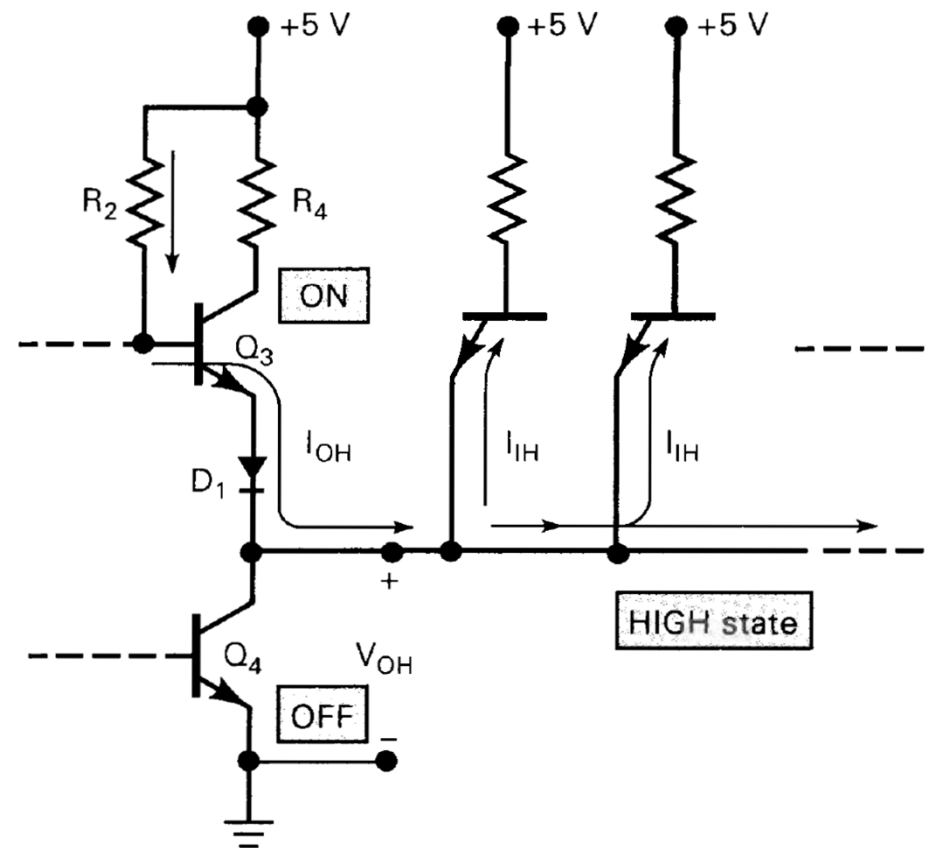
- Example: In datasheet of 74ALS00
 - $I_{OL}(\text{max}) = 8 \text{ mA}$, $I_{IL}(\text{max}) = 0.1 \text{ mA}$
 - $I_{OH}(\text{max}) = 0.4 \text{ mA} = 400 \mu\text{A}$, $I_{OL} = 20 \mu\text{A}$
 - **fan-out(LOW) = 80, fan-out(HIGH) = 20**

TTL Data Sheets

- Loading and Fan-out



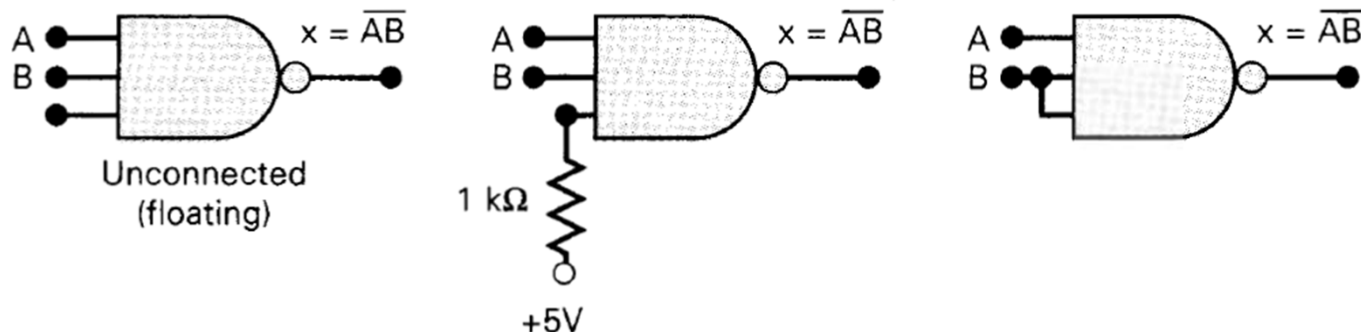
$$I_{OL} = \sum I_{IL}$$



$$I_{OH} = \sum I_{IH}$$

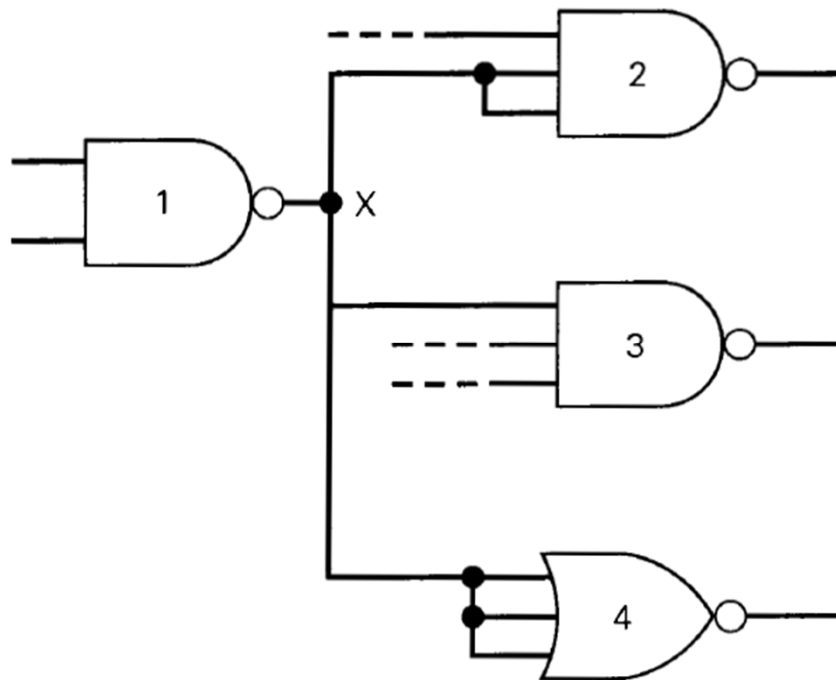
Other TTL Characteristics

- Unconnected Inputs (Floating)
 - Open input acts exactly like a logical 1 (HIGH)
- Unused Inputs
 - Left disconnected (undesirable – antenna)
 - Connect to V_{CC} (+5V) through a 1-k Ω resistor or to GND to produce for a constant-output logic level
 - Tied to a used input



Other TTL Characteristics

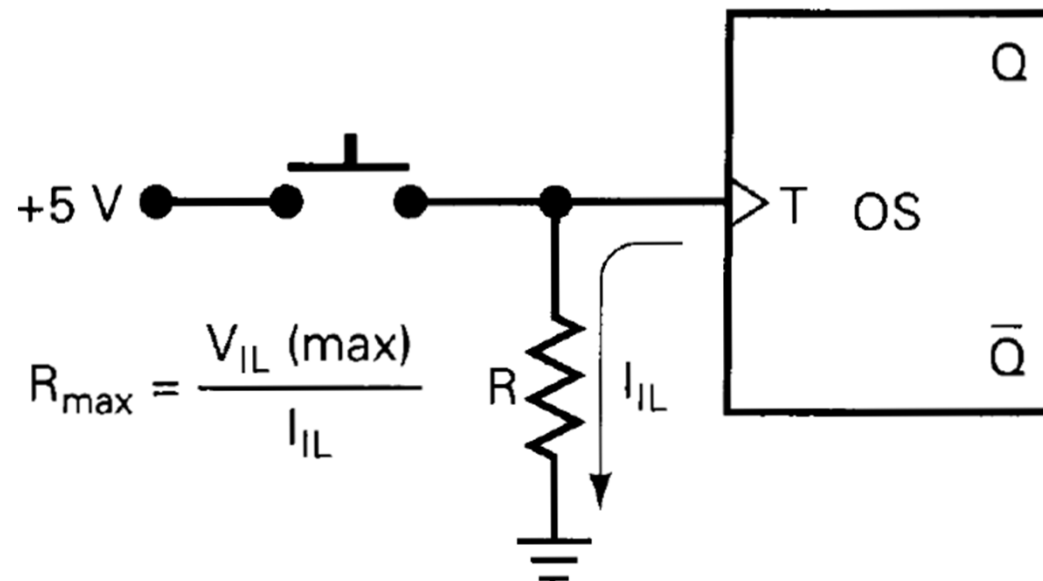
- Tied-Together Inputs
 - Represent a load – **Sum of the load current rating**
 - NAND, AND gates: LOW-state input load – **single input**



Loading on gate 1 output			
HIGH		LOW	
Load Current	Gate	Load Current	Gate
40 μ A	2	0.4 mA	2
20 μ A	3	0.4 mA	3
60 μ A	4	1.2 mA	4
120 μ A	Total	2.0 mA	Total

Other TTL Characteristics

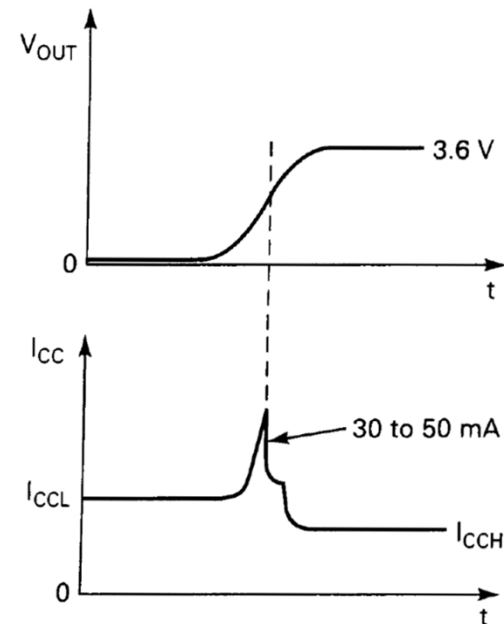
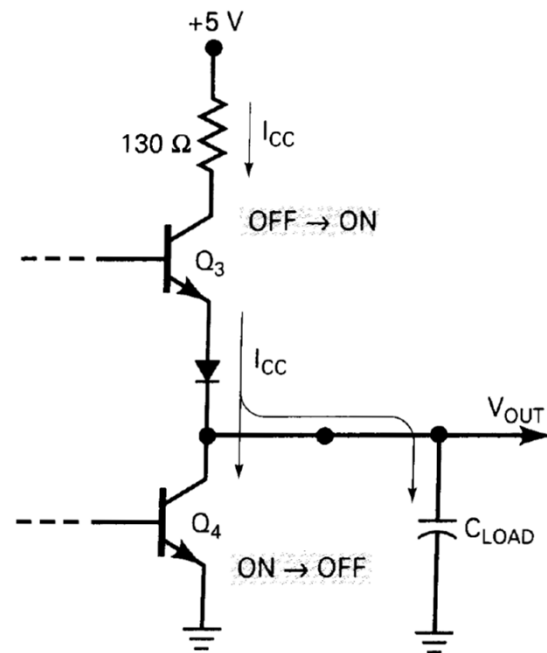
- Biasing TTL Inputs Low



Other TTL Characteristics

- Current Transients

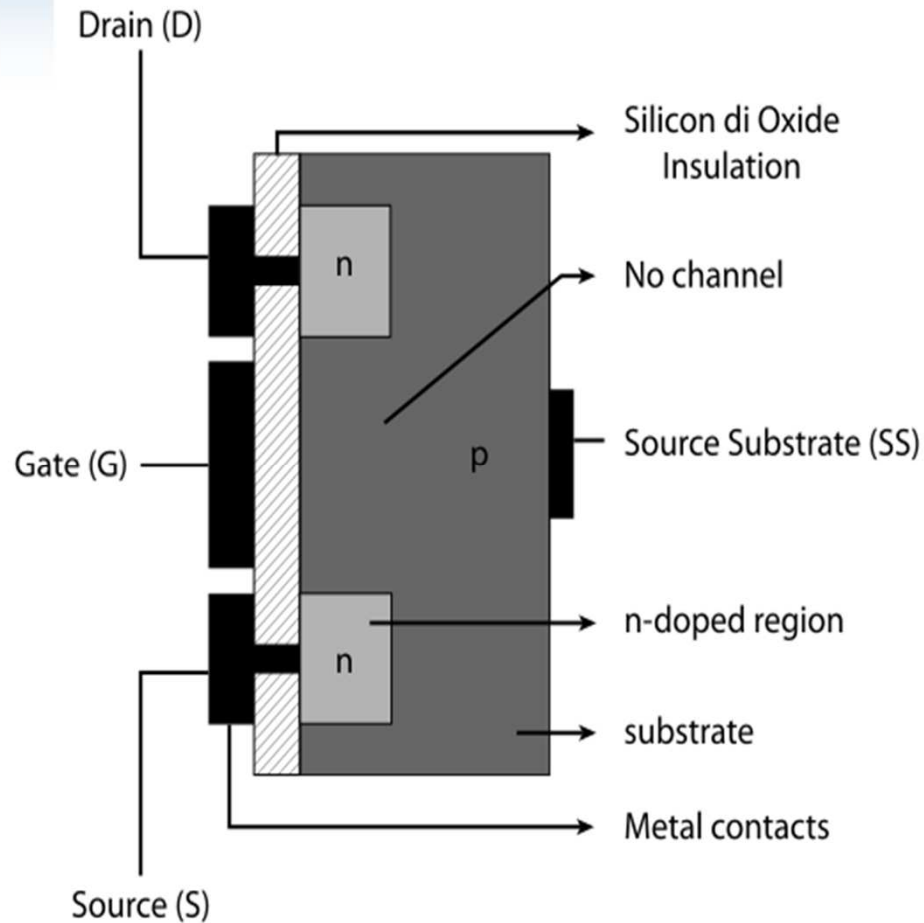
- high-amplitude current spike occurs when a totem-pole TTL output goes from LOW to HIGH
- **Power-supply decoupling:** capacitors connect from V_{CC} to GND ($0.01 \mu\text{F}$ or $0.1 \mu\text{F}$)



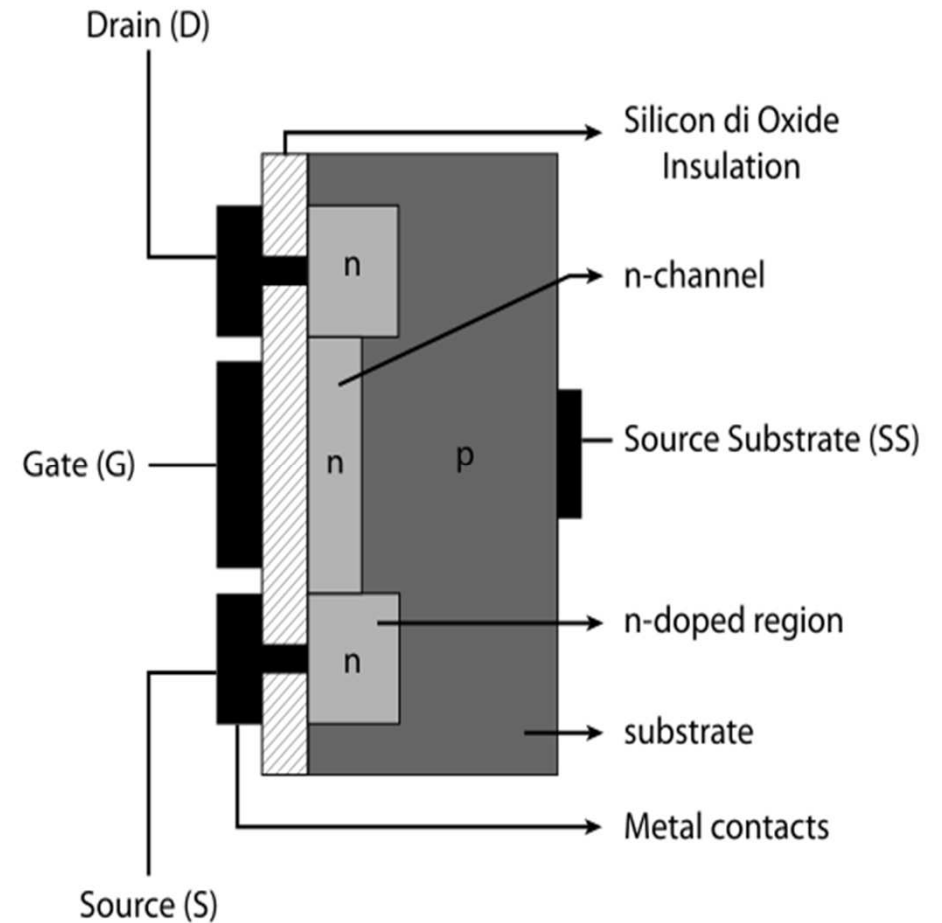
MOSFET

- Metal-oxide-semiconductor field-effect transistor
- Advantage
 - Simple, inexpensive to fabricate
 - Small, little power consumption
 - Suited for complex ICs
 - Faster than 74, 74LS, 74ALS TTL Series
- Disadvantage
 - susceptibility to static-electricity damage
- Depletion and enhancement MOSFET
 - http://www.electronics-tutorials.ws/transistor/tran_6.html

MOSFET Structure



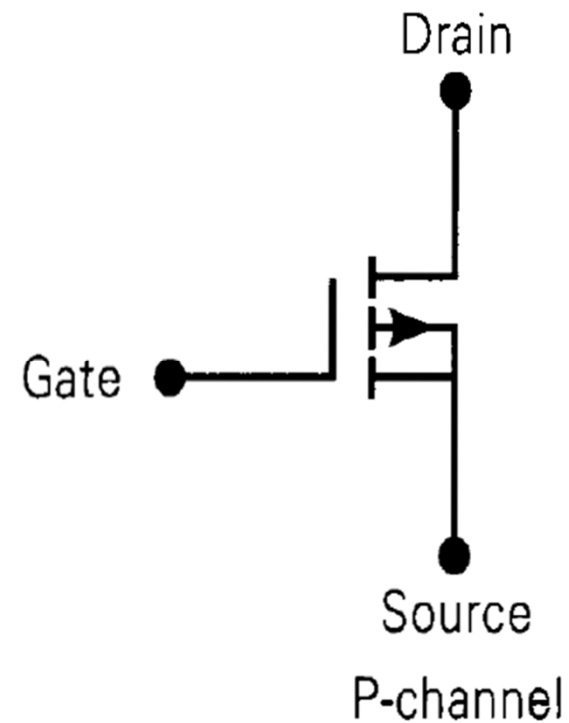
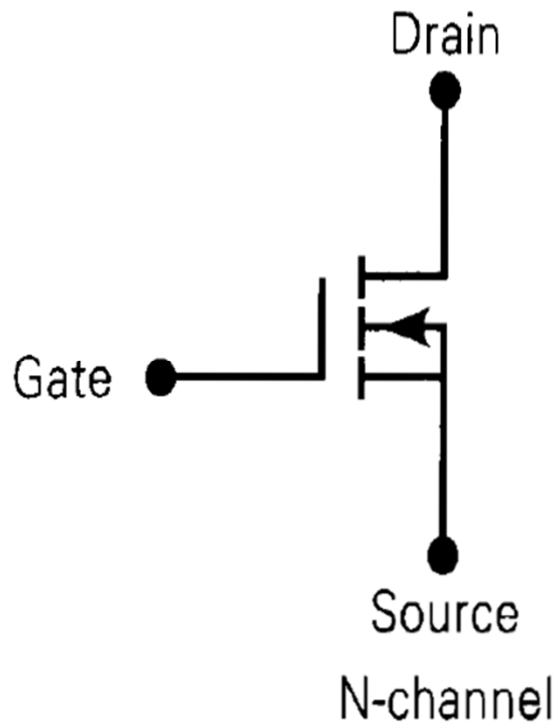
NMOS without channel
formed (**OFF state**)



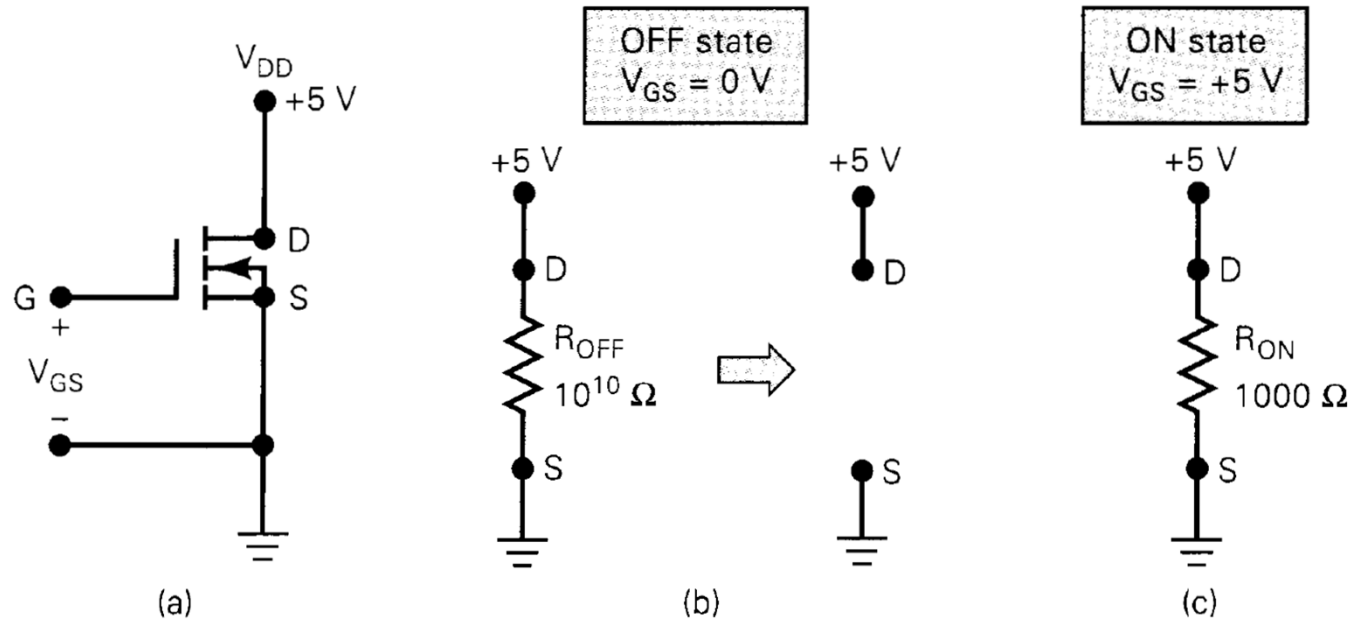
NMOS with channel
formed (**ON state**)

Enhancement MOSFET

- Use in digital ICs
- Enhancement MOSFET: normally “open” (OFF)



Basic MOSFET Switch

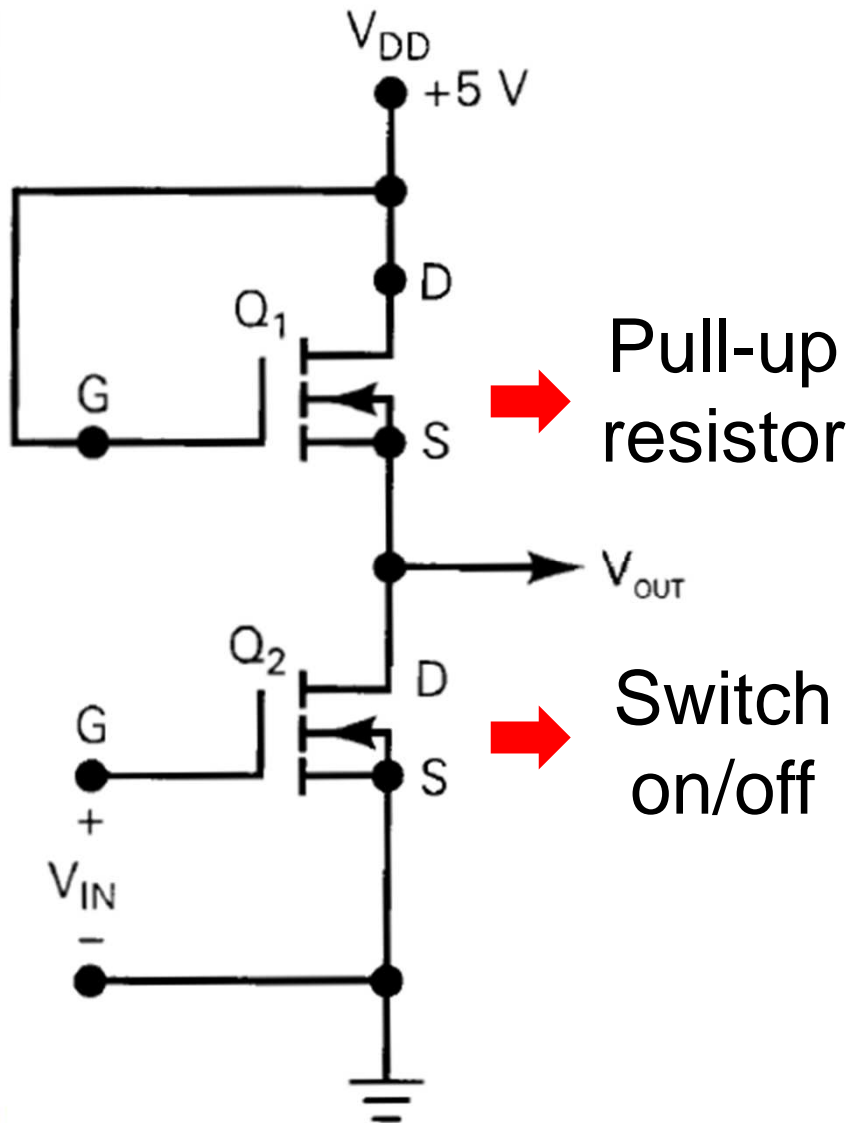


	Drain-to-Source Bias	Gate-to-Source Voltage (V_{GS}) Needed for Conduction	$R_{ON}\ (\Omega)$	$R_{OFF}\ (\Omega)$
P-channel	Negative	Typically more negative than -1.5 V	1000 (typical)	10^{10}
N-channel	Positive	Typically more positive than $+1.5\text{ V}$	1000 (typical)	10^{10}

Digital MOSFET Circuit

- N-MOS or P-MOS
 - Use MOSFET as a switch
 - Implement all resistors using channel resistance of a MOSFET
 - Simple circuits and fabrication processes
- C-MOS (complementary MOS)
 - Use both P- and N-channel MOSFET
 - Increase complexity of IC fabrication process, lower packing density
 - Faster and less power consumption

N-MOS Inverter

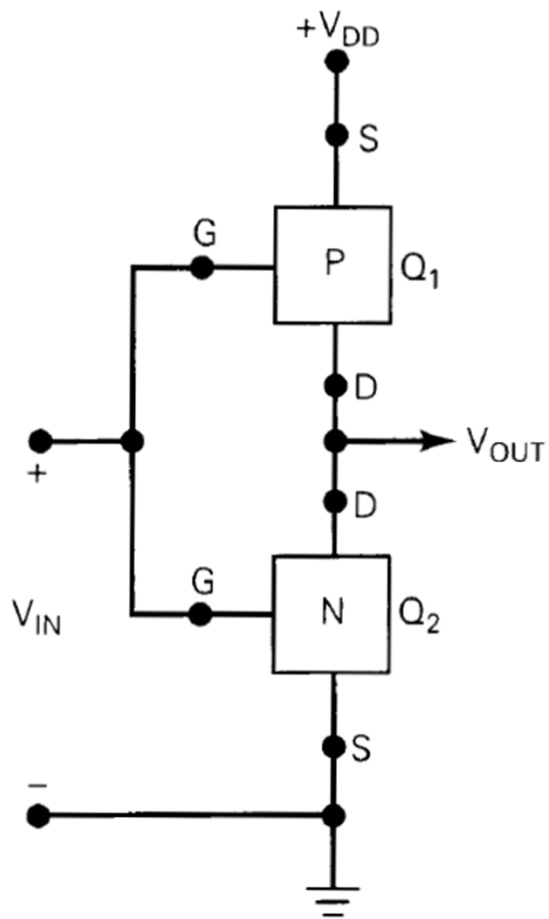


V_{IN}	Q_1	Q_2	$V_{OUT} = \overline{V_{IN}}$
0 V (logic 0)	$R_{ON} = 100\text{ k}\Omega$	$R_{OFF} = 10^{10}\text{ }\Omega$	+5 V (logic 1)
+5 V (logic 1)	$R_{ON} = 100\text{ k}\Omega$	$R_{ON} = 1\text{ k}\Omega$	+0.05 V (logic 0)

- Gate of Q_1 connected to the drain \rightarrow always ON
 \rightarrow pull-up resistor $100\text{ k}\Omega$

Complementary MOS Logic

- CMOS Inverter

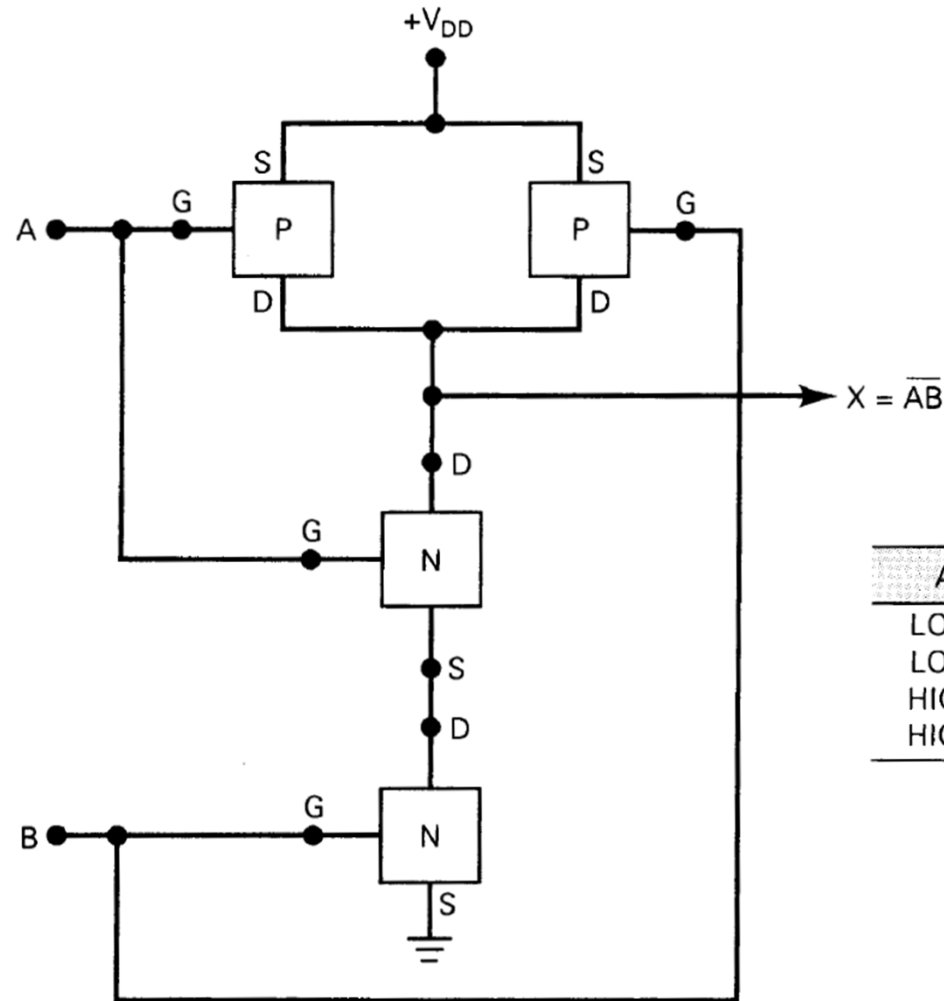


V_{IN}	Q_1	Q_2	V_{OUT}
$+V_{DD}$ (logic 1)	OFF $R_{OFF} = 10^{10} \Omega$	ON $R_{ON} = 1 \text{ k}\Omega$	$\approx 0 \text{ V}$
0 V (logic 0)	ON $R_{ON} = 1 \text{ k}\Omega$	OFF $R_{OFF} = 10^{10} \Omega$	$\approx +V_{DD}$

$$V_{OUT} = \overline{V_{IN}}$$

Complementary MOS Logic

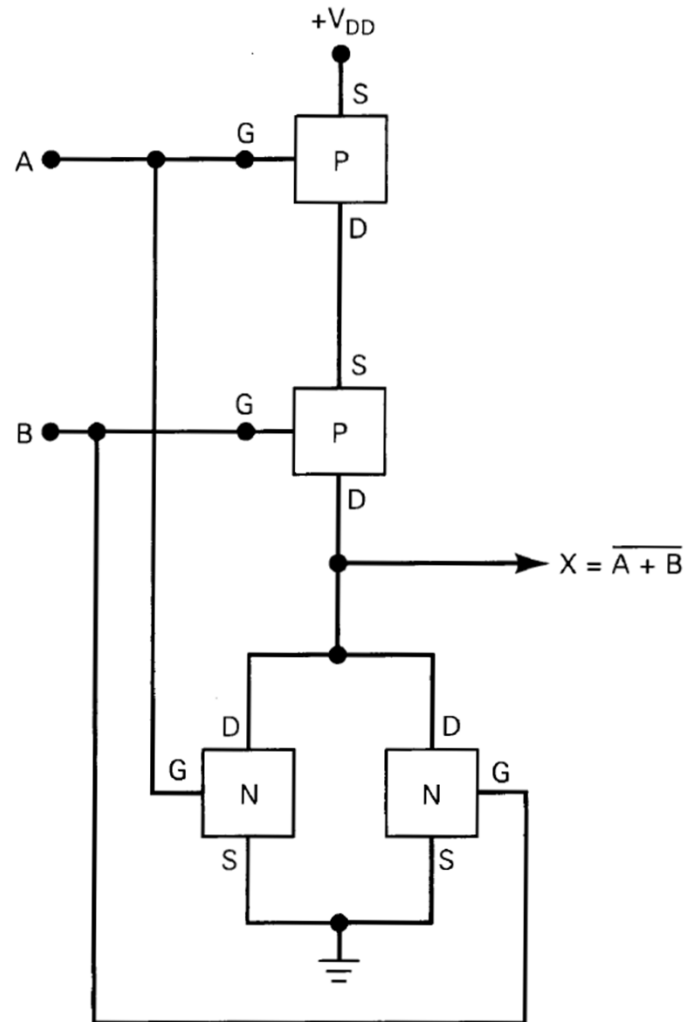
- CMOS NAND Gate



A	B	X
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

Complementary MOS Logic

- CMOS NOR Gate



A	B	X
LOW	LOW	HIGH
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	LOW

CMOS Series

- 4000/14000 Series
- 74C Series
- 74HC/HCT (*High-Speed CMOS*)
- 74AC/ACT (*Advanced CMOS*)
- 74AHC/74AHCT (*Advanced High-Speed CMOS*)
- BICMOS 5-Volt Logic

Low-Voltage Technology

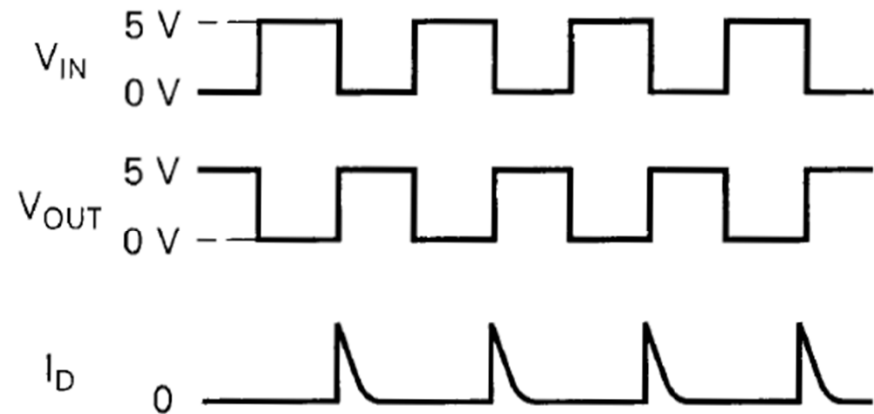
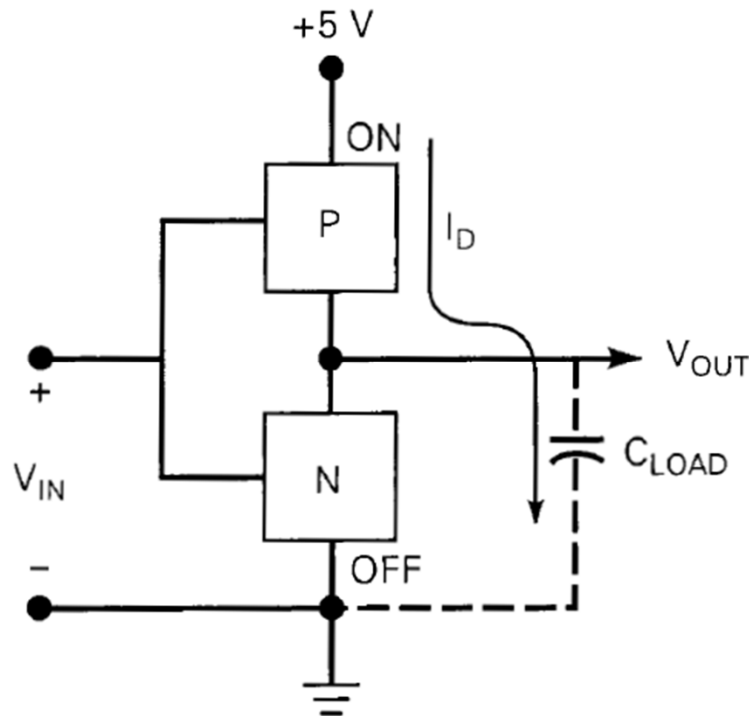
- CMOS Family
 - 74LVC (*Low-Voltage CMOS*)
 - 74ALVC (*Advanced Low-Voltage CMOS*)
 - 74LV (*Low-Voltage*)
 - 74AVC (*Advanced Very-Low-Voltage CMOS*)
- BiCMOS Family
 - 74LVT (*Low-Voltage BiCMOS Technology*)
 - 74LVT (*Advanced Low-Voltage BiCMOS Technology*)
 - 74ALB (*Advanced Low-Voltage BiCMOS*)

CMOS Characteristics (1)

- Power-Supply Voltage (V_{DD}): 3-15V
- Logic Voltage Levels
 - Not sink/source any significant amount of current
 - V_{OL} : close to 0 V, V_{OH} : close to V_{DD}
- Noise Margins: greater than TTL
 - $V_{NH} = V_{OH}(\min) - V_{IH}(\min)$
 - $V_{NL} = V_{IL}(\max) - V_{OL}(\max)$
- Power Dissipation
 - Extremely low (high resistance) → Suitable for applications using battery power

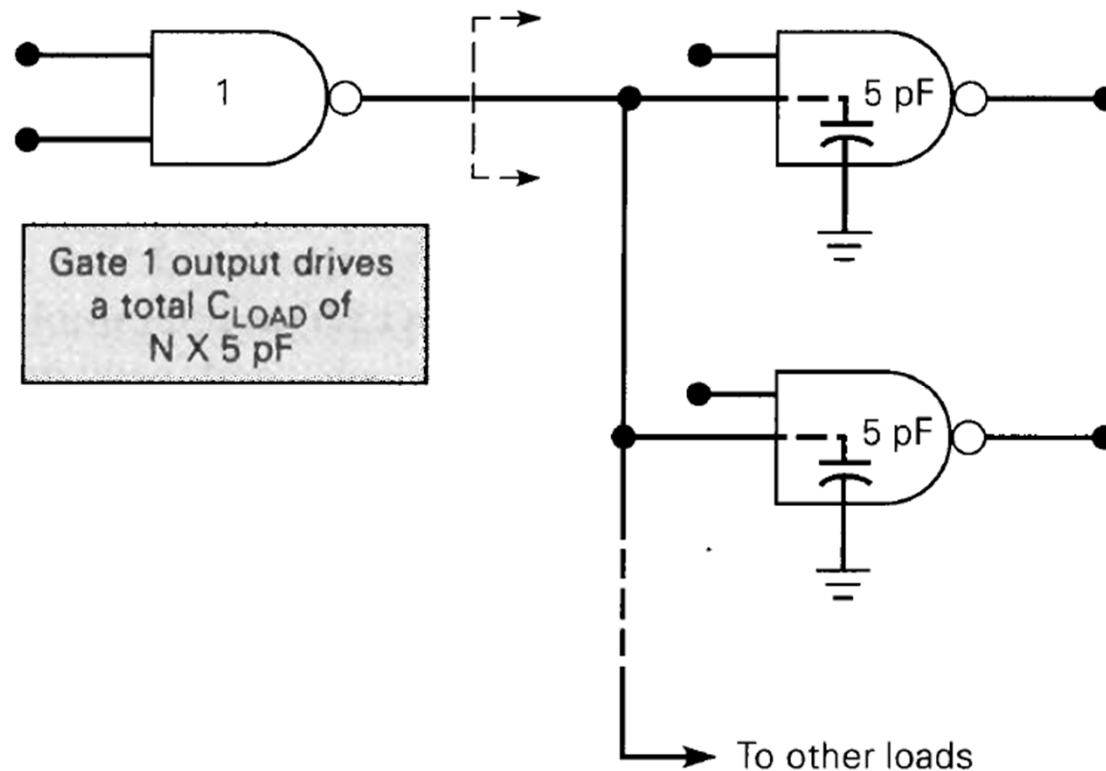
CMOS Characteristics (2)

- P_D increases with Frequency
 - Increase in proportion to the frequency at switching states of the circuit (LOW to HIGH)



CMOS Characteristics (3)

- Fan-Out: depend on
 - Permissible maximum propagation delay
 - Frequency ???

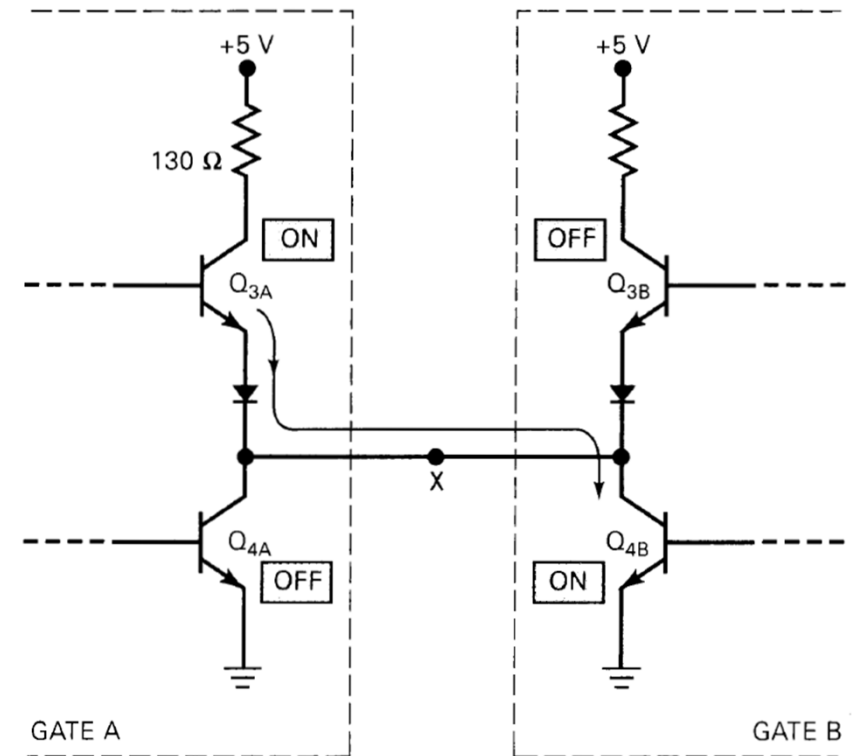
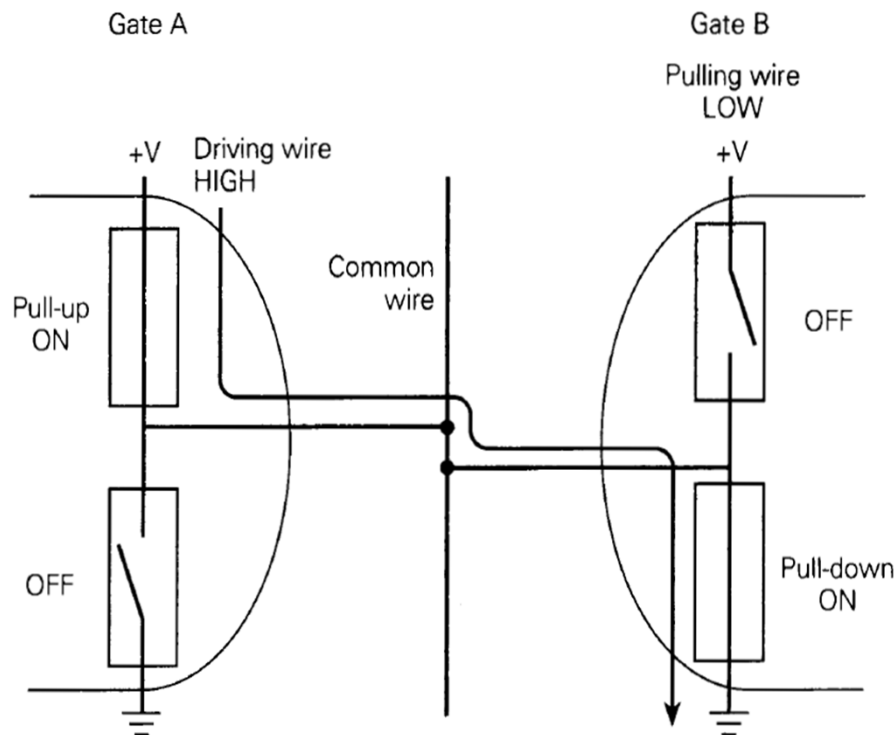


CMOS Characteristics (4)

- Switching Speed
 - Faster than N-MOS and P-MOS (low output resistance
 - 1 k Ω vs. 100 k Ω)
- Unused Inputs
 - **Never left disconnected** : susceptible to noise and static charges
 - Tie to fixed voltage level (0V or V_{DD}) or to another input
- Static Sensitivity
- Latch-Up
 - Transistors stay ON permanently
 - Solution: Clamping diodes

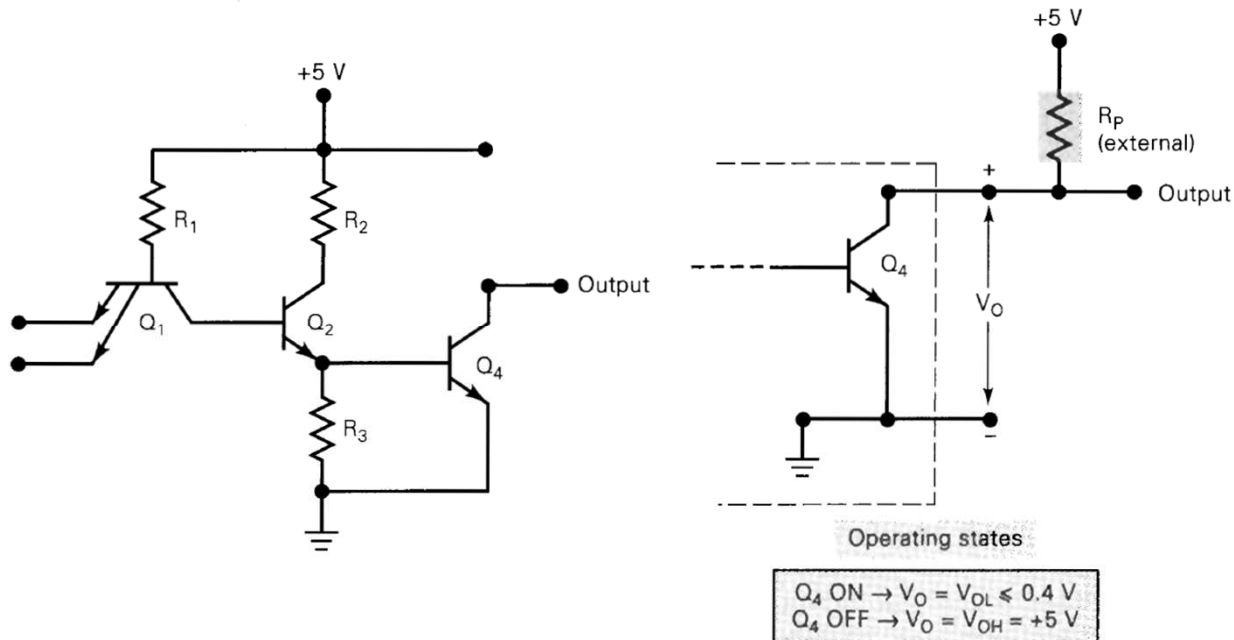
Output Combination (sharing a common wire)

- Conventional CMOS outputs, TTL totem pole outputs should **never be tied together**
 - Output voltage: in the indeterminate range
 - Damage the ICs (high current)

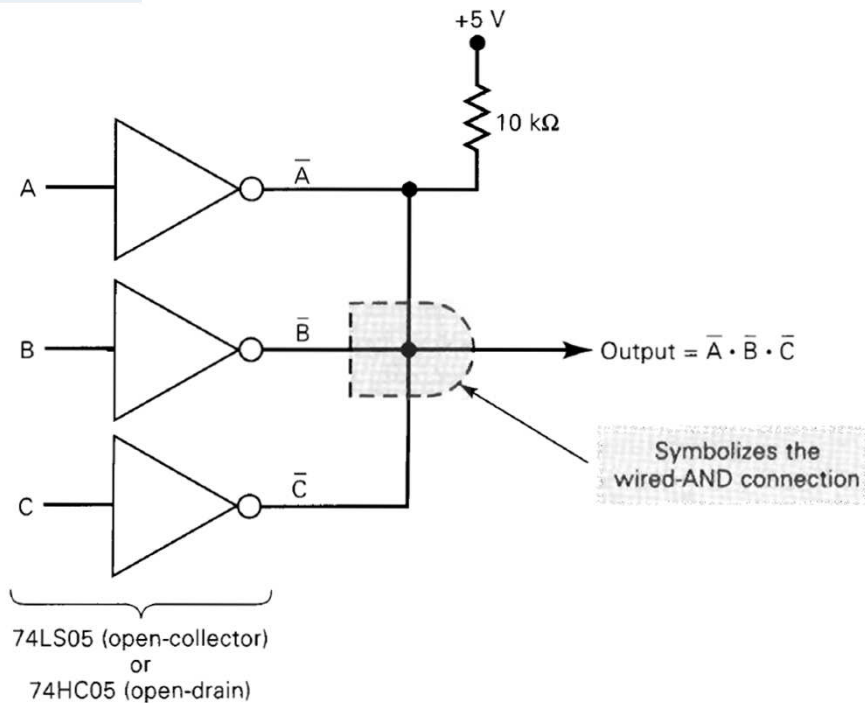


Open-Collector/Open-Drain Outputs

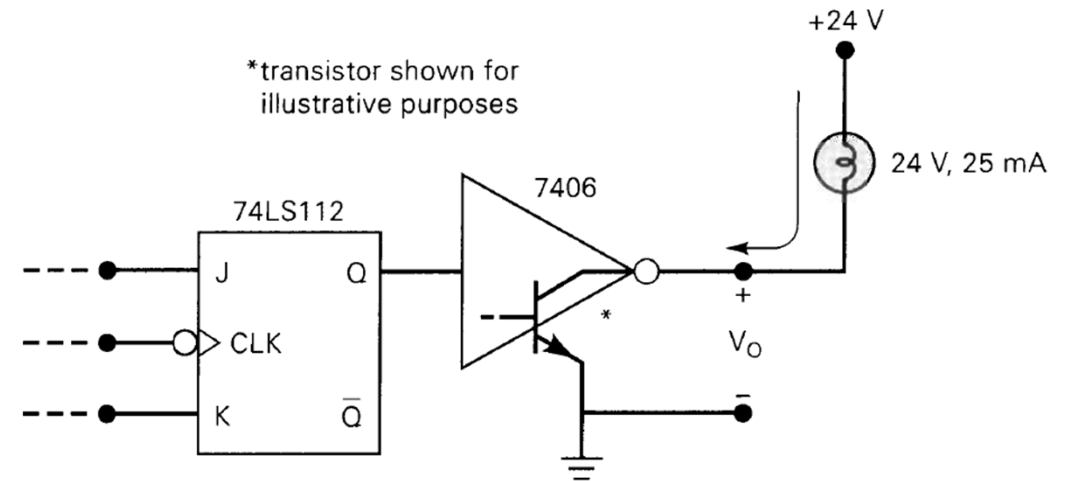
- Solution: **remove** the *active pull-up transistor*
 - CMOS output circuits: **open-drain outputs**
 - TTL totem pole output circuit: **open-collector outputs**
 - Output LOW state: no problem
 - Output HIGH state: *external pull-up resistor R_p*



Open-collector/drain outputs Application



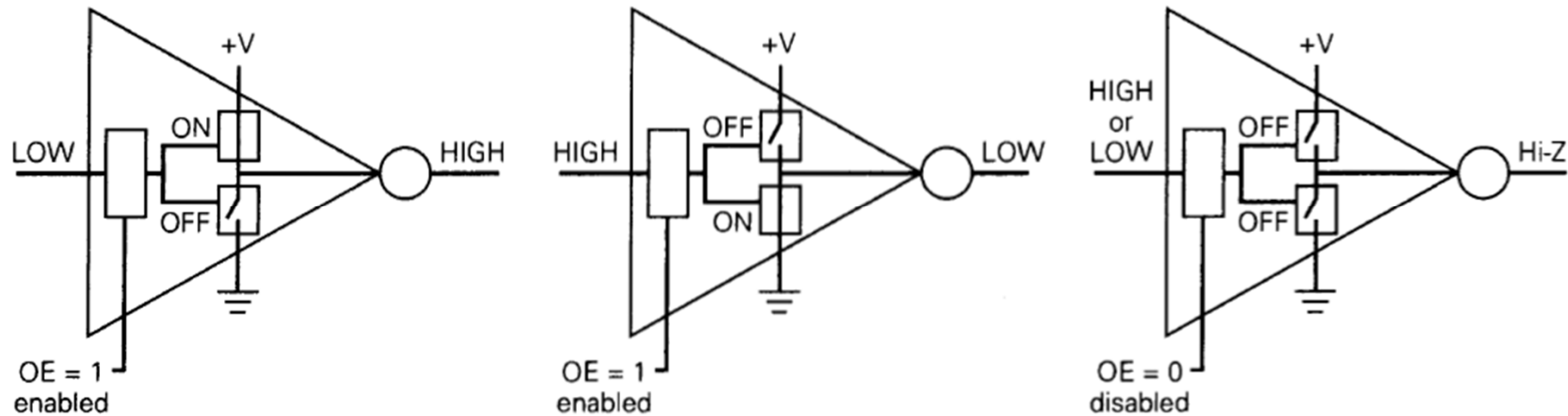
Wired-AND
connection



Open-collector/drain
Buffer/Driver

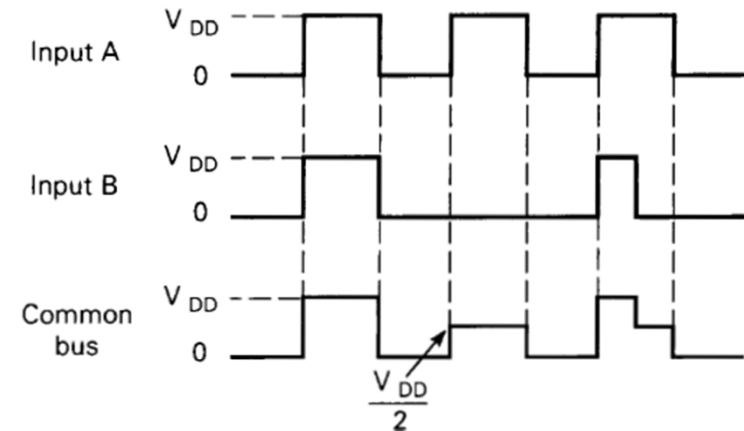
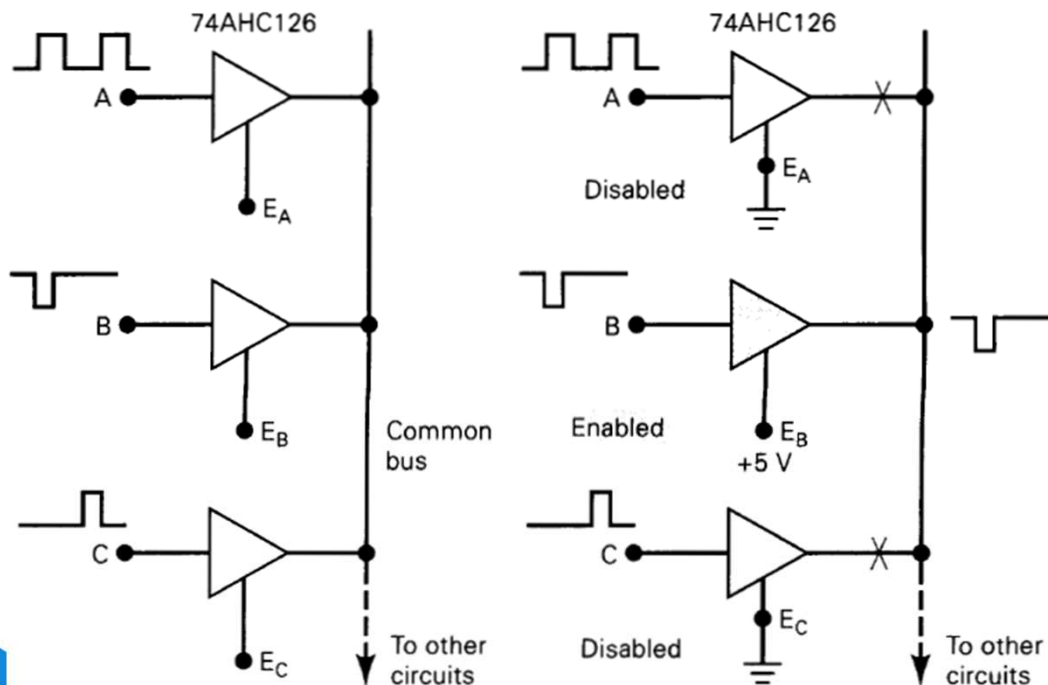
Tristate (Three-State) Logic Outputs

- Allow three possible output states:
 - HIGH, LOW
 - High-impedance (Hi-Z): both pull-up and pull-down transistors are turned OFF
- Have an *enable* input (OE – output enable)



Tristate (Three-State) Logic Outputs

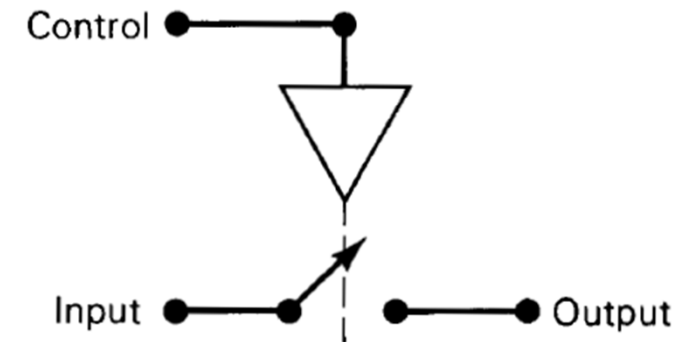
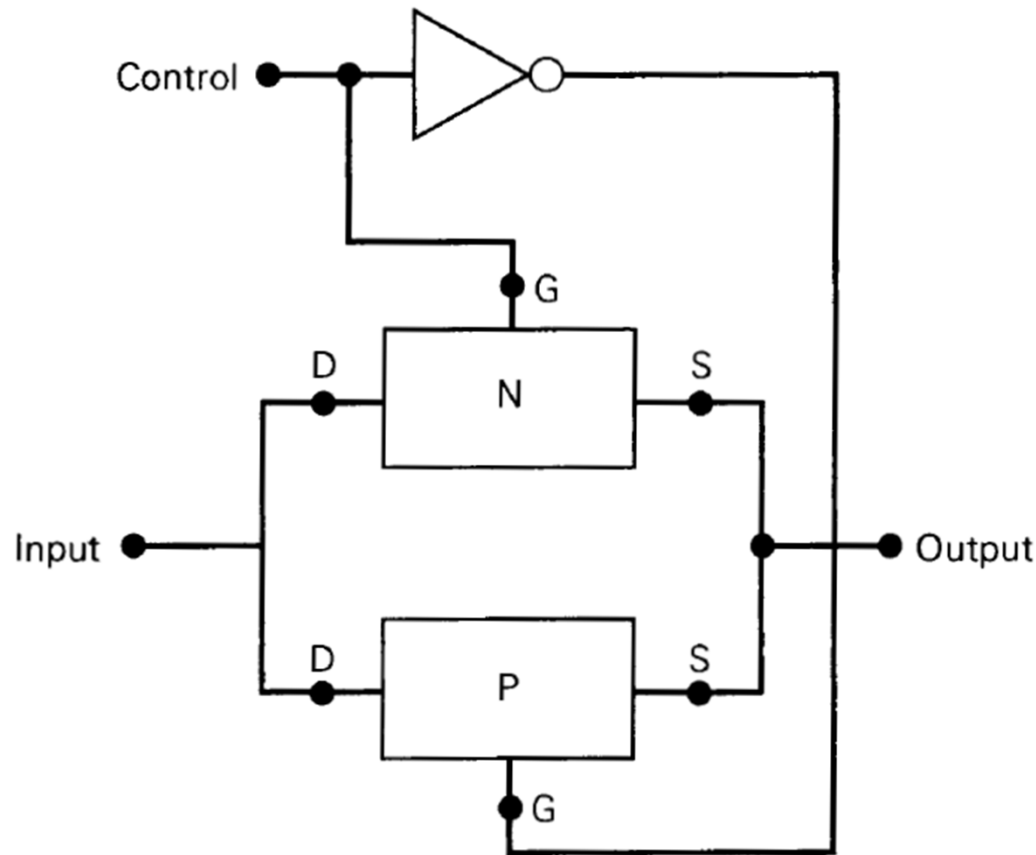
- Advantage
 - Tristate ICs output can be connected together
 - Low-impedance, high-speed characteristic
- Application: Tristate Buffers



Bus contention

CMOS Transmission Gate (Bilateral Switch)

- Pass signals in both directions
- Digital and analog applications



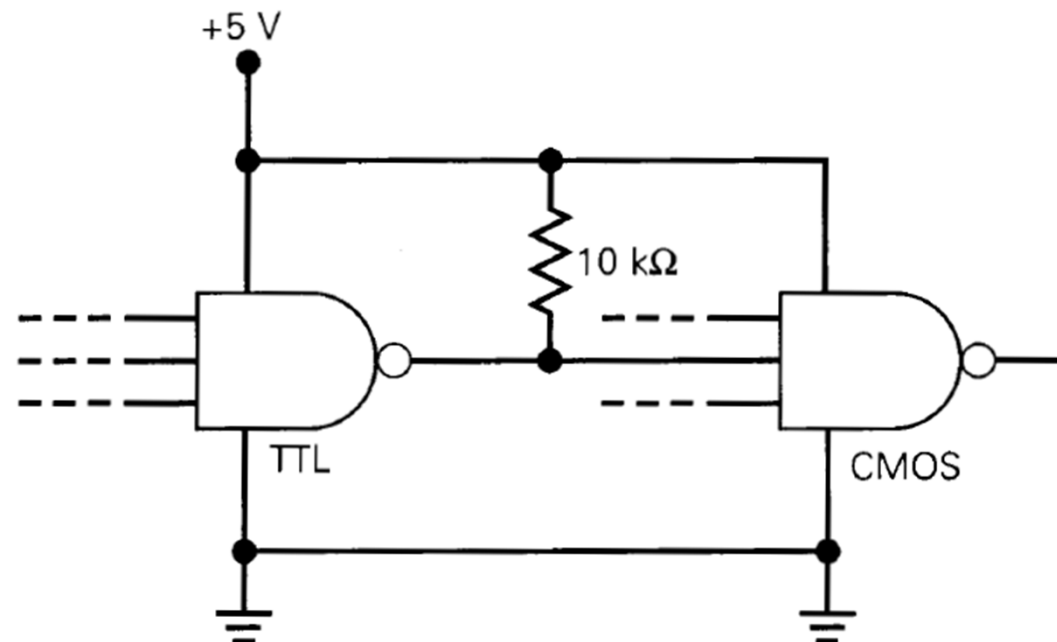
Control input	Switch
0 V	Open (OFF)
+V _{DD}	Closed (ON)

IC Interfacing

- Connecting the output(s) to the input(s) of different electrical characteristic systems.
- Take advantage of the strong points of each IC family
 - High-speed, greater output current/voltage capability, high frequency
- Concerned problems
 - Fan-out
 - Voltage and current parameters

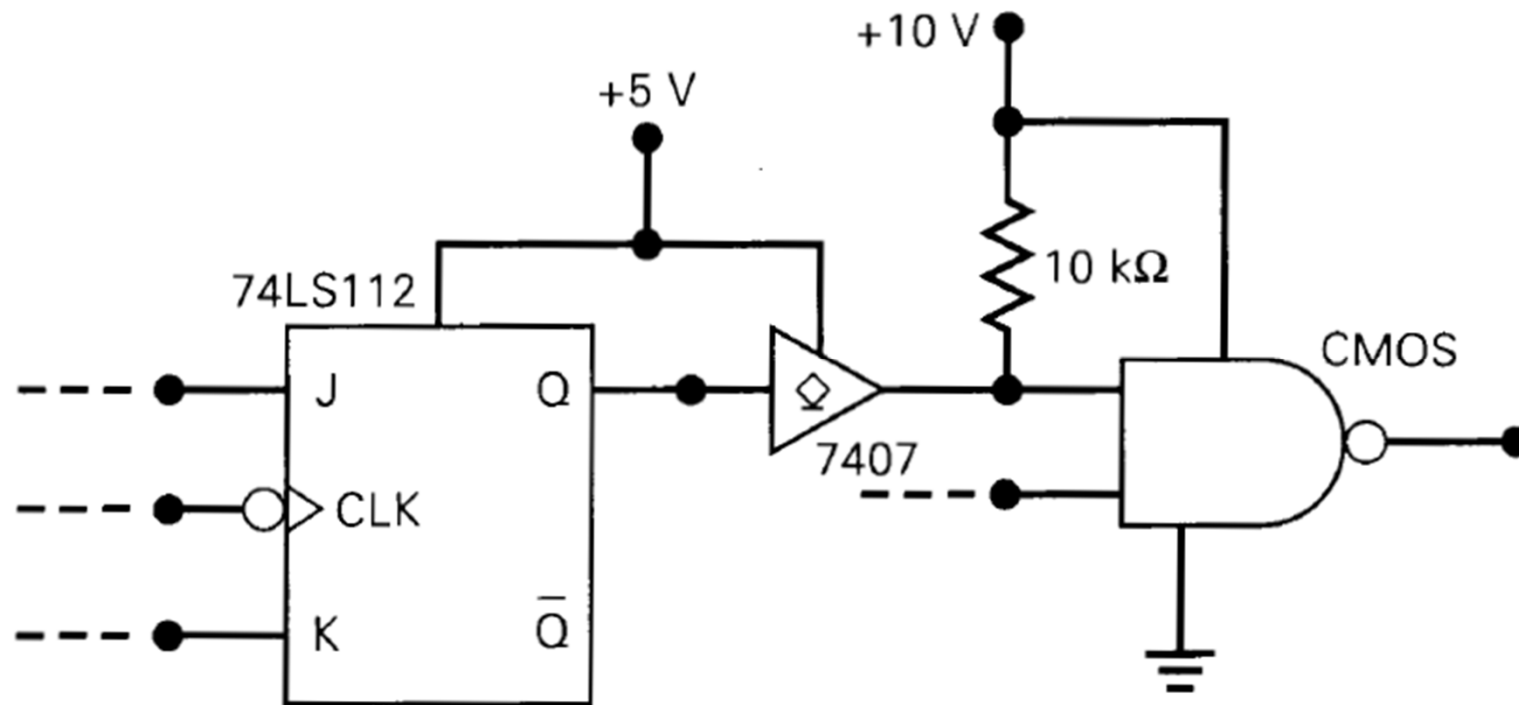
TTL Driving CMOS

- Current: no problem
- Output voltages
 - $V_{OH}(\text{min})$ of TTL: too low when compared with $V_{IH}(\text{min})$ of CMOS
 - Solution: *Pull-up resistor* at TTL output



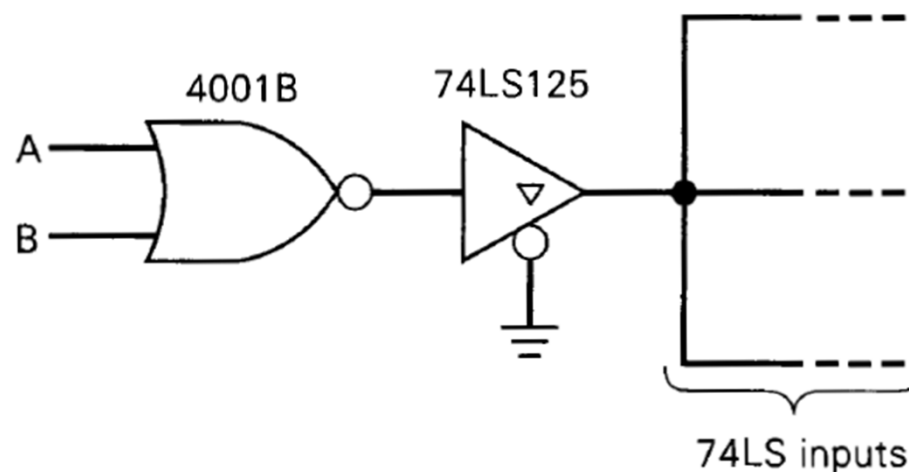
TTL Driving CMOS

- Driving High-Voltage CMOS
 - Use TTL series from certain manufacturers that can operate with an high-voltage output pull-up
 - Utilize a **voltage level-translator**



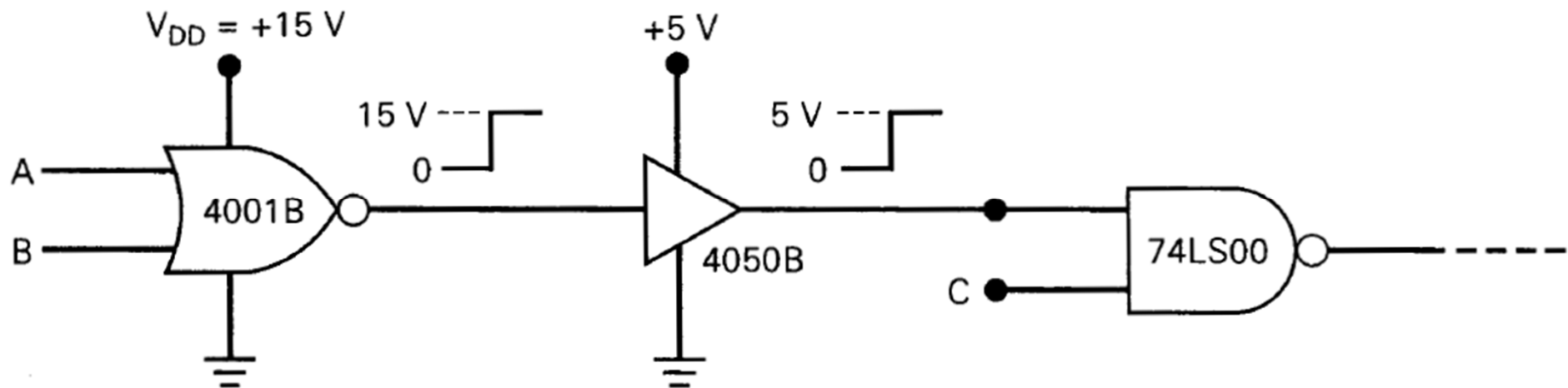
CMOS Driving TTL

- Driving TTL in the HIGH State: no problem
- Driving TTL in the LOW State:
 - Excepting 4000B series, 74HC/74HCT series have no trouble driving a single TTL load of any series
 - Concern fan-out problem
 - Use buffer to interface low-current CMOS to high-current TTL



CMOS Driving TTL

- High-Voltage CMOS Driving TTL
 - Use TTL series that can withstand high-voltage input
 - Use voltage level-translator



Reference

- Chapter 8, Digital System – Principles and Applications, Ronald J.Tocci, Neal S. Widmer