



# Chapter 3

# INTERFACING WITH THE

# ANALOG WORLD



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# LOGIC DESIGN 2

MSI logic circuits

Memory

**ADC / DAC**

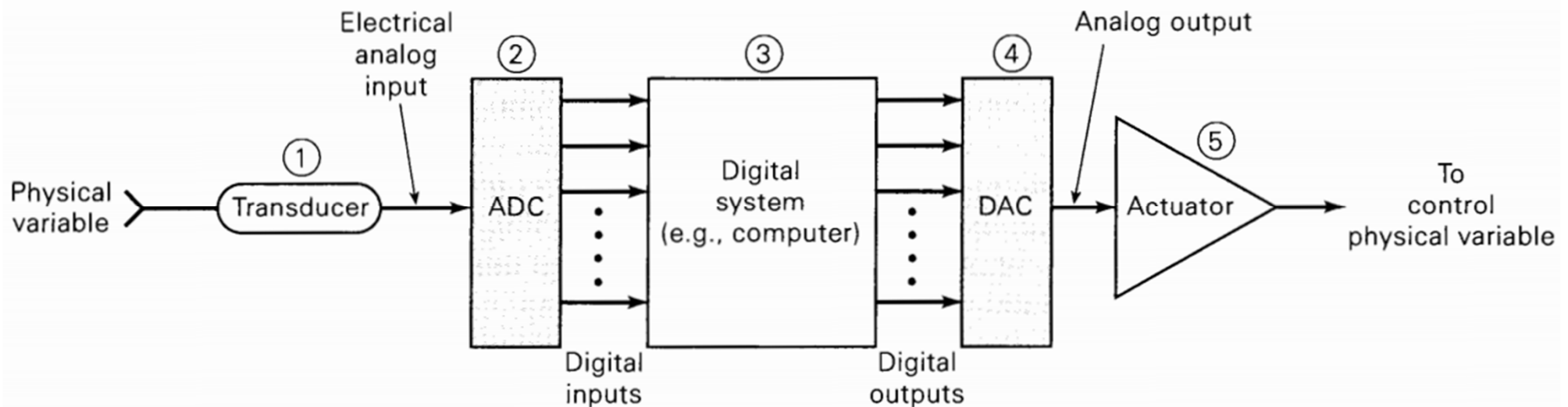
Logic family

# Digital vs. Analog

- Digital quantity
  - Value: 0 or 1, LOW or HIGH, true or false, ...
  - Digital circuits respond in the same way to all voltage values within a given range
    - Example:  $0 - 0.8 \text{ V} \rightarrow \text{logic 0}$   
 $2 - 5 \text{ V} \rightarrow \text{logic 1}$
- Analog quantity
  - Take on any value over a continuous range of values
  - Exactly value is significant, each possible value has a different meaning
  - Example: temperature, pressure, audio signals, ...

# Interfacing with the Analog World

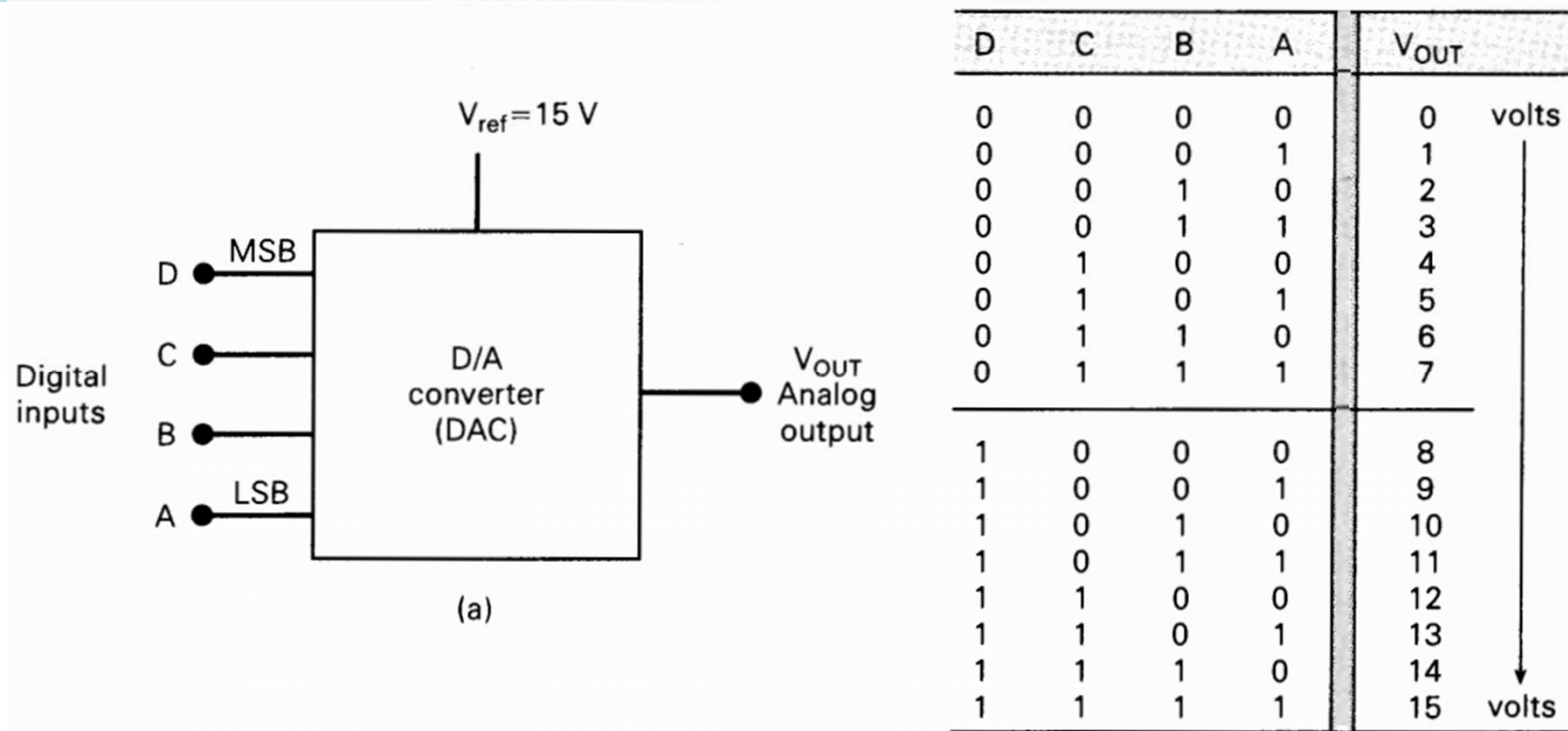
- Any information that inputted to a digital system must first be put into digital form
- To monitor/control a physical variable by digital outputs → must deal with the difference between the digital nature and the analog nature



# Interfacing with the Analog World

- **Transducer:** convert the physical variable to an electrical variable
  - Electrical output is an analog current or voltage
- **Analog-to-digital converter (ADC):** convert analog input to digital outputs
- **Computer**
- **Digital-to-analog converter (DAC):** convert digital outputs to proportional analog voltage or current
- **Actuator:** device/circuit to control the physical variable

# Digital-to-Analog Conversion



- $V_{ref}$ : voltage reference  $\rightarrow$  determine the **full-scale output** (maximum value that DAC can produce)

$$\text{analog output} = K \times \text{digital input}$$

$K$ : proportional factor (voltage/current units)

# Digital-to-Analog Conversion

- **Example 1:** 4-input DAC has voltage output
  - $V_{ref} = 15 \text{ V}$ , largest input:  $1111_2 = 15_{10} \rightarrow K = 1 \text{ V}$

With a digital input of  $1100_2 = 12_{10}$

→ Output voltage:  $V_{OUT} = (1 \text{ V}) \times 12 = 12 \text{ V}$

- **Example 2:** 5-input DAC has current output
  - Digital input  $10100_2 = 20_{10} \rightarrow$  output current is 10 mA
  - $I_{OUT} = ?$  for a digital input of  $11101_2$

$I_{OUT} = K \times \text{digital input} \rightarrow 10 \text{ mA} = K \times 20 \rightarrow K = 0.5 \text{ mA}$

With a digital input of  $11101_2 = 29_{10}$

→ Output voltage:  $I_{OUT} = (0.5 \text{ mA}) \times 29 = 14.5 \text{ mA}$

# Analog Output

- The output of a DAC is technically not an analog quantity because it can take on only specific values
- Increase the number of input bits will
  - Increase the number of different possible output values
  - Decrease the different between successive values



# Input Weights

- Each digital input contributes a different amount to the analog output
  - The contributions of each digital input are *weighted* according to their position in the binary number

- Example: 5-bit DAC

- Input of 00001  $\rightarrow V_{OUT} = 0.2 \text{ V}$

- Input of 11111  $\rightarrow V_{OUT} = ?$

0.2 V is the weight of the LSB

$\rightarrow$  The weights of other bits:

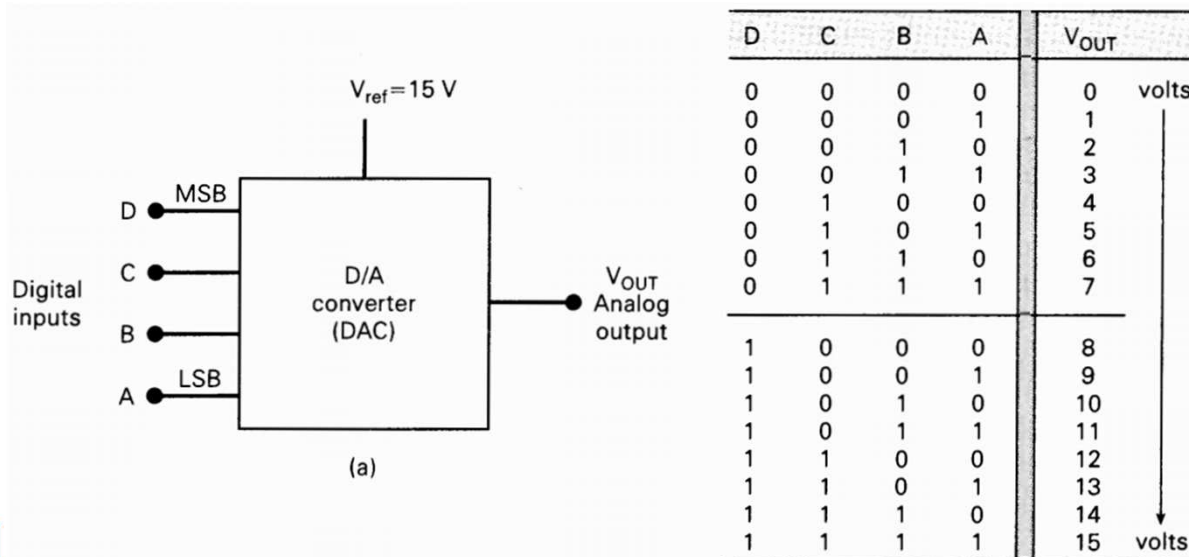
0.4 V, 0.8 V, 1.6 V and 3.2 V

$\rightarrow V_{OUT} = 3.2 + 1.6 + 0.8 + 0.4 + 0.2 = 6.2 \text{ (V)}$

D	C	B	A		$V_{OUT} \text{ (V)}$
0	0	0	1	$\rightarrow$	1
0	0	1	0	$\rightarrow$	2
0	1	0	0	$\rightarrow$	4
1	0	0	0	$\rightarrow$	8

# Resolution (Step size)

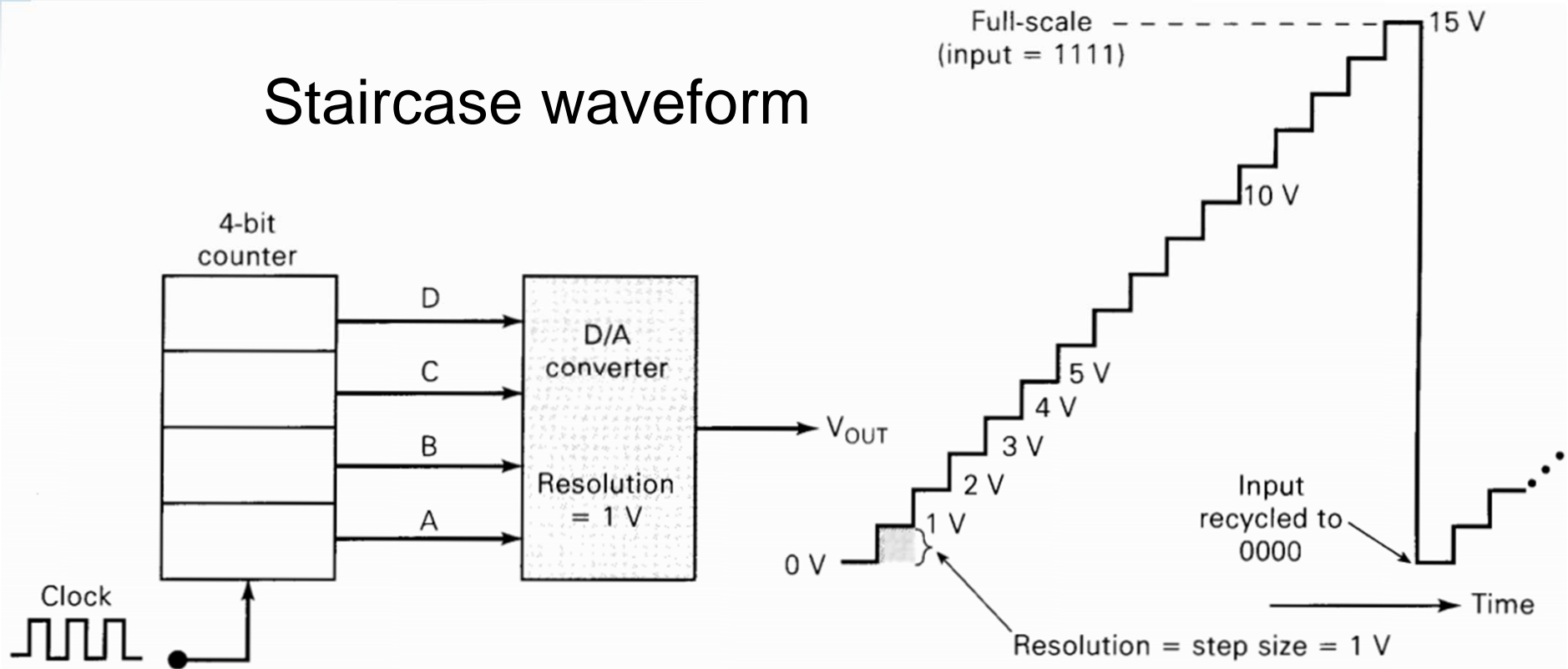
- **Resolution** of a DAC is defined as the *smallest change* that can occur in the analog output as a result of a change in the digital input
  - Resolution is always *equal* to the *weight of the LSB*
  - Referred to as the **step size** (the different between one step to the next)



➡ **Resolution = 1 V**

# Resolution (Step size)

## Staircase waveform



$$\text{Resolution} = K = \text{step size} = \frac{A_{fs}}{(2^n - 1)}$$

$A_{fs}$ : the analog **full-scale** output

$n$  : the number of bits  $\rightarrow$  number of steps:  $(2^n - 1)$

# Resolution (Step size)

- Percentage Resolution

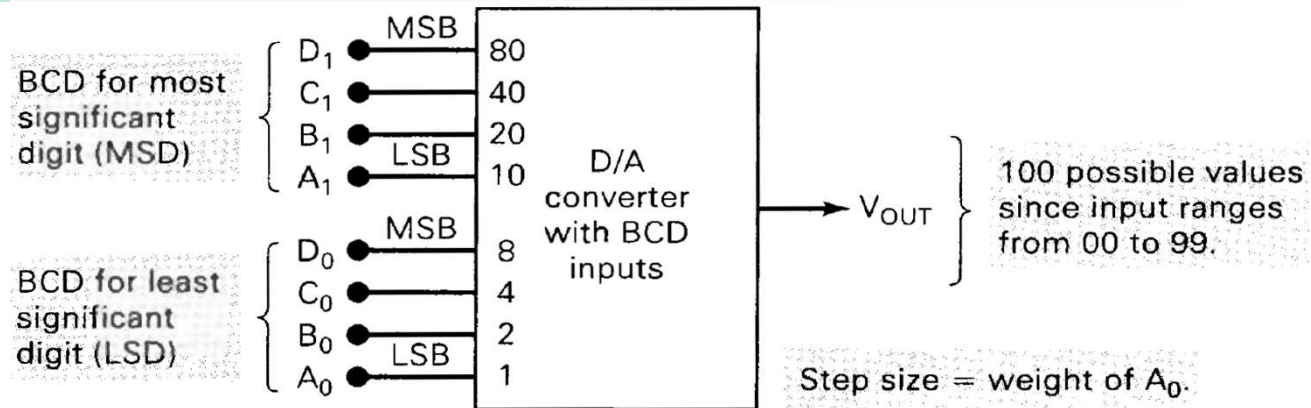
$$\% \text{ resolution} = \frac{\text{step size}}{\text{full scale (F.S.)}} \times 100\%$$

$$\% \text{ resolution} = \frac{1}{\text{total number of steps}} \times 100\%$$

$$N\text{-bit DAC, total number of steps} = 2^N - 1$$

- The resolution limits how close the DAC output can come to a given analog value
  - The cost of DACs increases with the number of bits
  - Use only as many bits as necessary

# BCD Input Code



- Example:
  - The weight of  $A_0$  is 0.1 V  $\rightarrow$  *step size* = 0.1 V
  - Input ranges from 00 to 99  $\rightarrow$  *number of steps* = 99  
 $\rightarrow$  *Full-scale output* =  $99 \times 0.1 = 9.9$  V
  - $D_1C_1B_1A_1 = 0101$  and  $D_0C_0B_0A_0 = 1000 \rightarrow$  Input code: **58**<sub>10</sub>  
 $\rightarrow V_{OUT} = (0.1 \text{ V}) \times 58 = 5.8 \text{ V}$

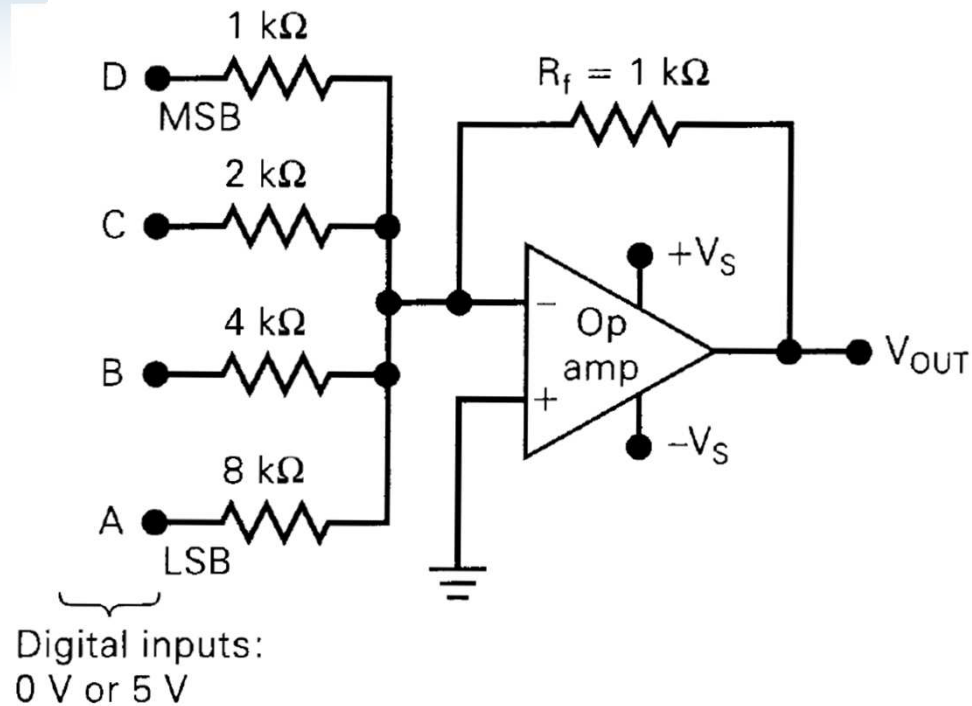
MSD				LSD			
$D_1$	$C_1$	$B_1$	$A_1$	$D_0$	$C_0$	$B_0$	$A_0$
8.0	4.0	2.0	1.0	0.8	0.4	0.2	0.1

$$V_{OUT} = \overbrace{4}^{C_1} \text{ V} + \overbrace{1}^{A_1} \text{ V} + \overbrace{0.8}^{D_0} \text{ V} = 5.8 \text{ V}$$

# Bipolar DACs

- Produce both negative and positive values
- Negative input values are represented in 2's-complement form
- Number of steps is  $2^n - 1$
- Example: 6-bit bipolar DAC
  - Uses the 2's-complement system
  - Resolution = 0.2 V
  - Number of steps: 63 ( $2^6 - 1$ )
  - Binary input values: 100000 (-32) to 011111 (+31)  
Analog outputs: – 6.4 to +6.2 V

# D/A-Converter Circuitry



$R_f$ : feedback resistor

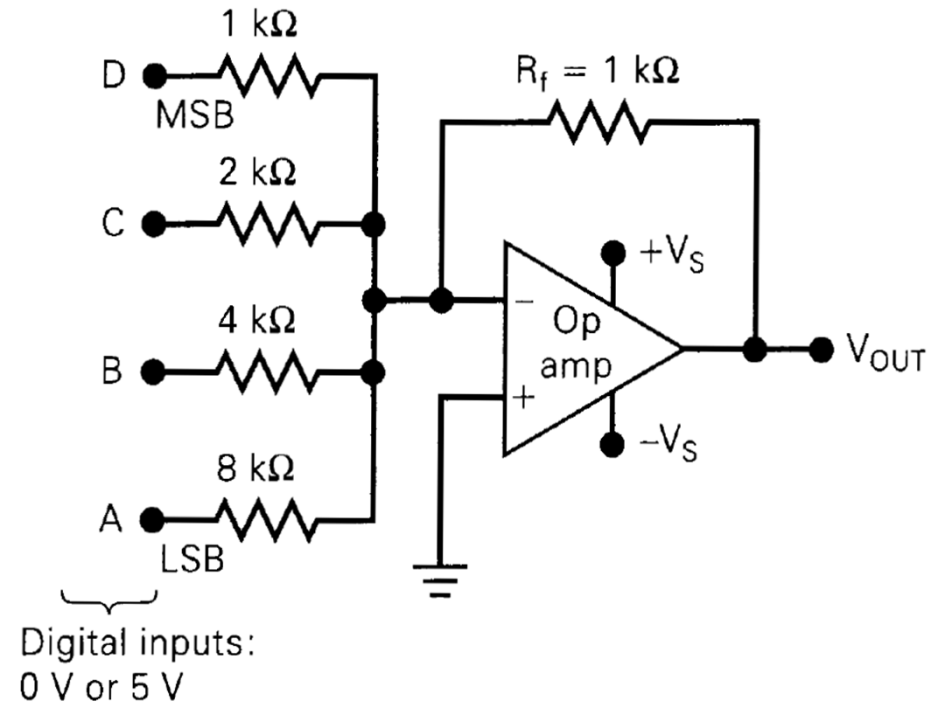
- $R_{IN} = R_f \rightarrow$  no attenuation
- $R_{IN} = 2R_f \rightarrow$  attenuated by  $1/2$

$$V_{OUT} = - (V_D + 1/2 V_C + 1/4 V_B + 1/8 V_A)$$

Input code				$V_{OUT}$ (volts)
D	C	B	A	
0	0	0	0	0
0	0	0	1	-0.625 ← LSB
0	0	1	0	-1.250
0	0	1	1	-1.875
0	1	0	0	-2.500
0	1	0	1	-3.125
0	1	1	0	-3.750
0	1	1	1	-4.375
1	0	0	0	-5.000
1	0	0	1	-5.625
1	0	1	0	-6.250
1	0	1	1	-6.875
1	1	0	0	-7.500
1	1	0	1	-8.125
1	1	1	0	-8.750
1	1	1	1	-9.375 ← Full-scale

# D/A-Converter Circuitry

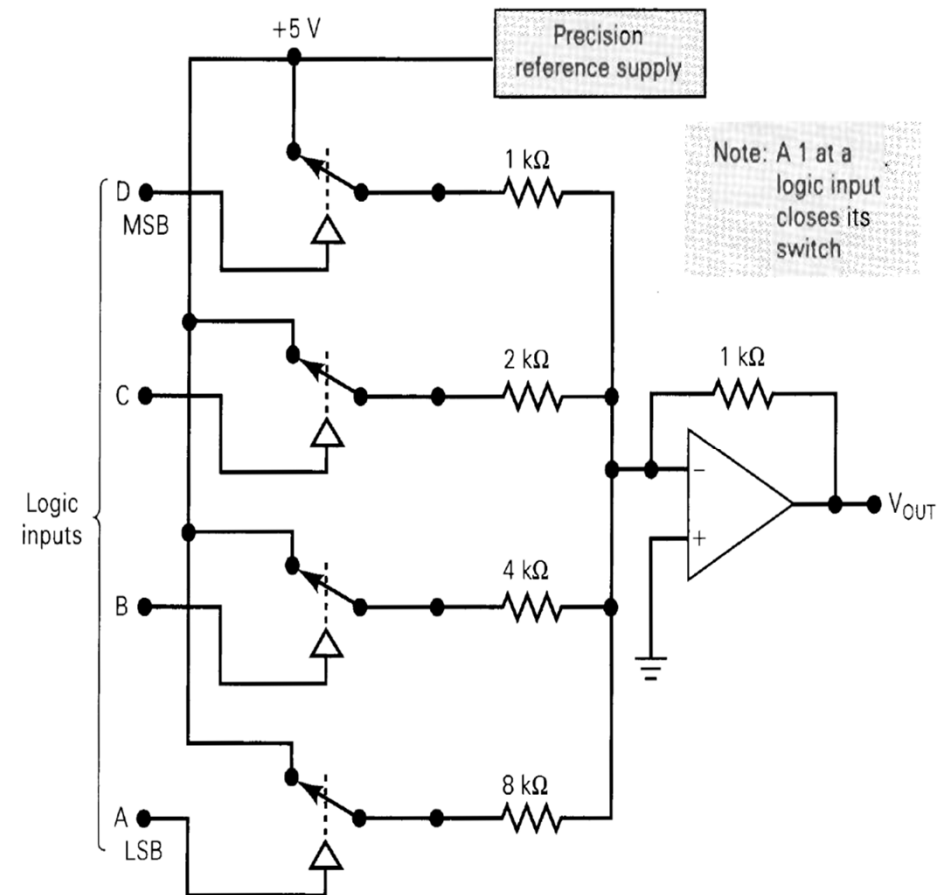
- Example
  - MSB  $\rightarrow 5V$
  - 2<sup>nd</sup> MSB  $\rightarrow 2.5V$
  - 3<sup>rd</sup> MSB  $\rightarrow 1.25V$
  - LSB  $\rightarrow 0.625V$
  - If  $R_f = 250\Omega \rightarrow$  each input weight will be four times smaller



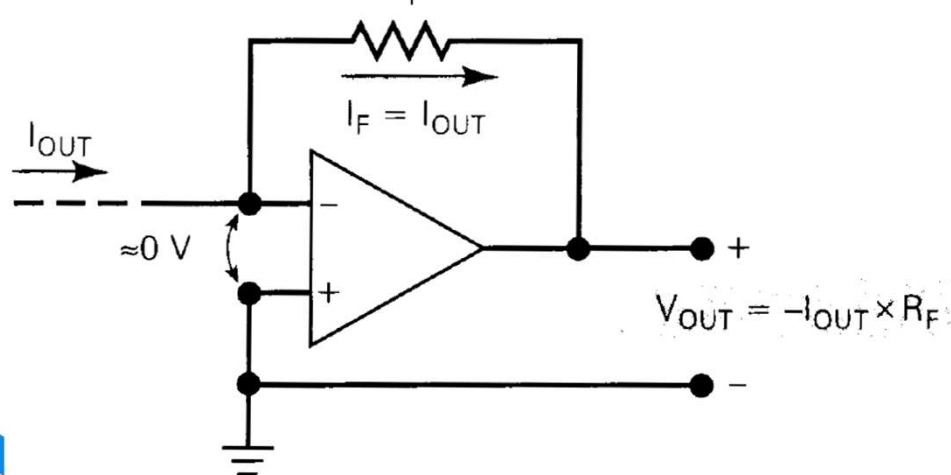
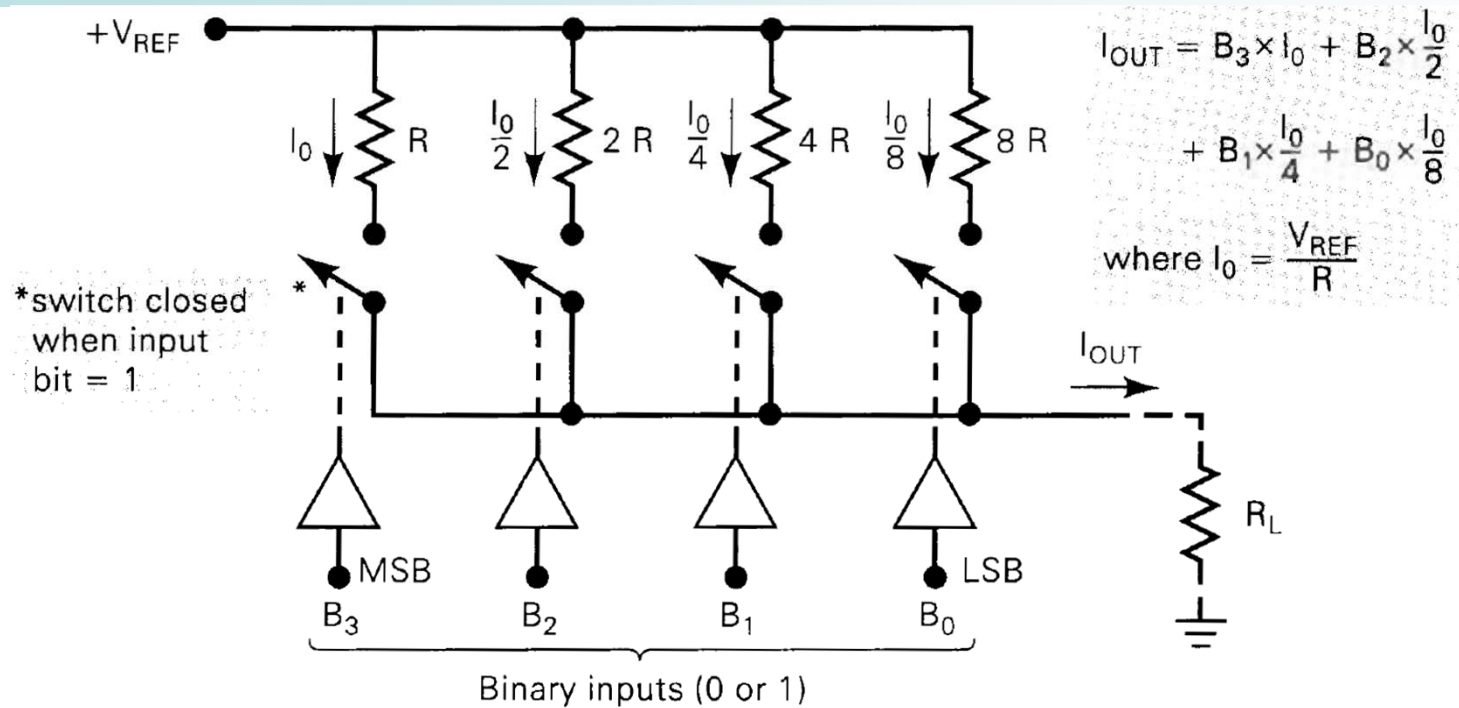


# Conversion Accuracy

- Depends primarily on 2 factors
  - the precision of the input and feedback resistors
  - the precision of the input voltage levels
- *Precision reference supply*
  - Produces a very stable, precise voltage needed to generate an accurate analog output



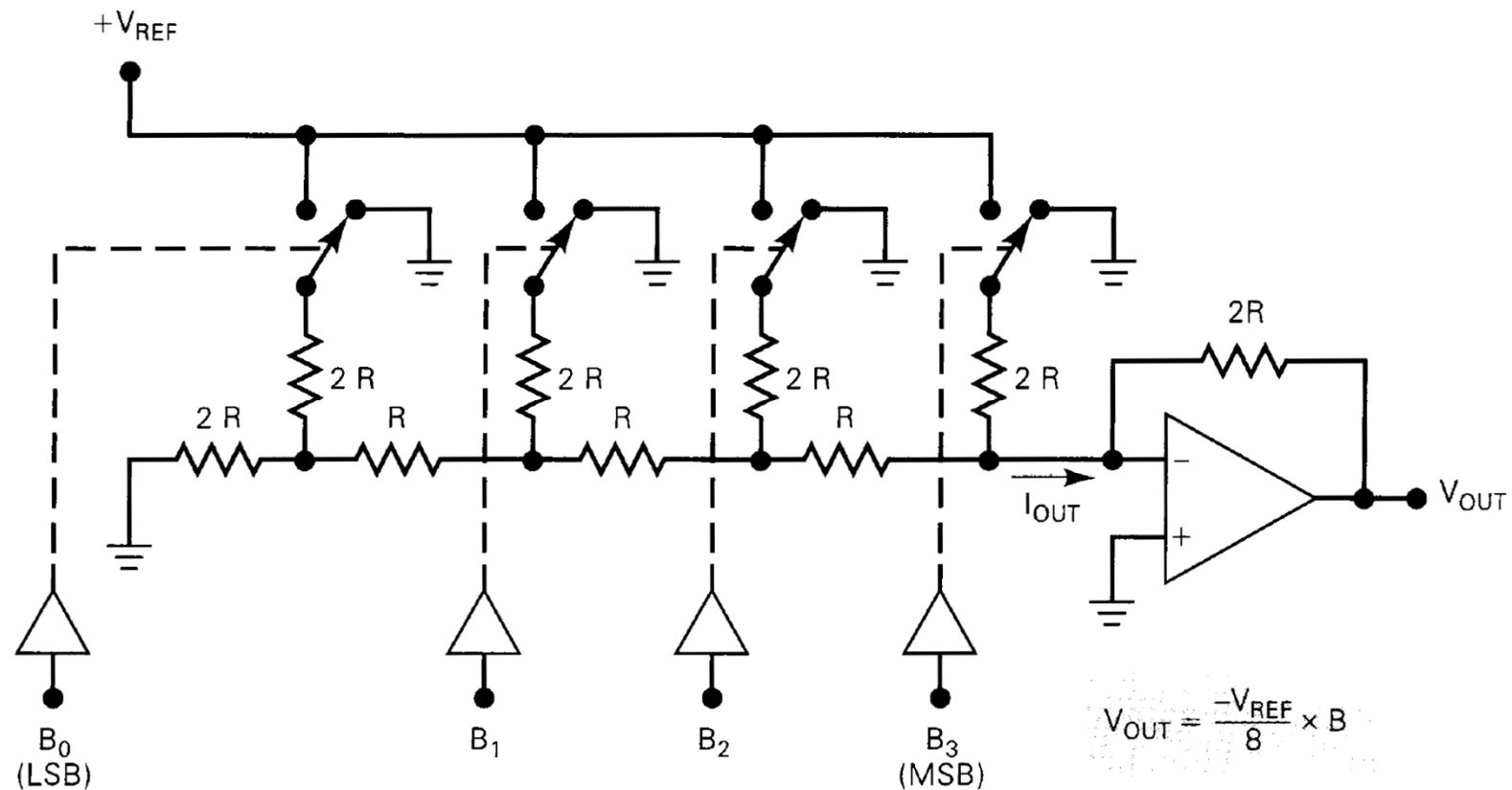
# DAC with Current Output



$R_L$ : much smaller than  $R$

For  $I_{OUT}$  to be accurate  
 $\rightarrow$  use op-amp as a *current-to-voltage* converter

# R/2R Ladder



$$V_{OUT} = -(V_{REF} / 8) \times B$$

*B: the value of binary input*

<http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/dac.html#c3>

# DAC Specifications (1)

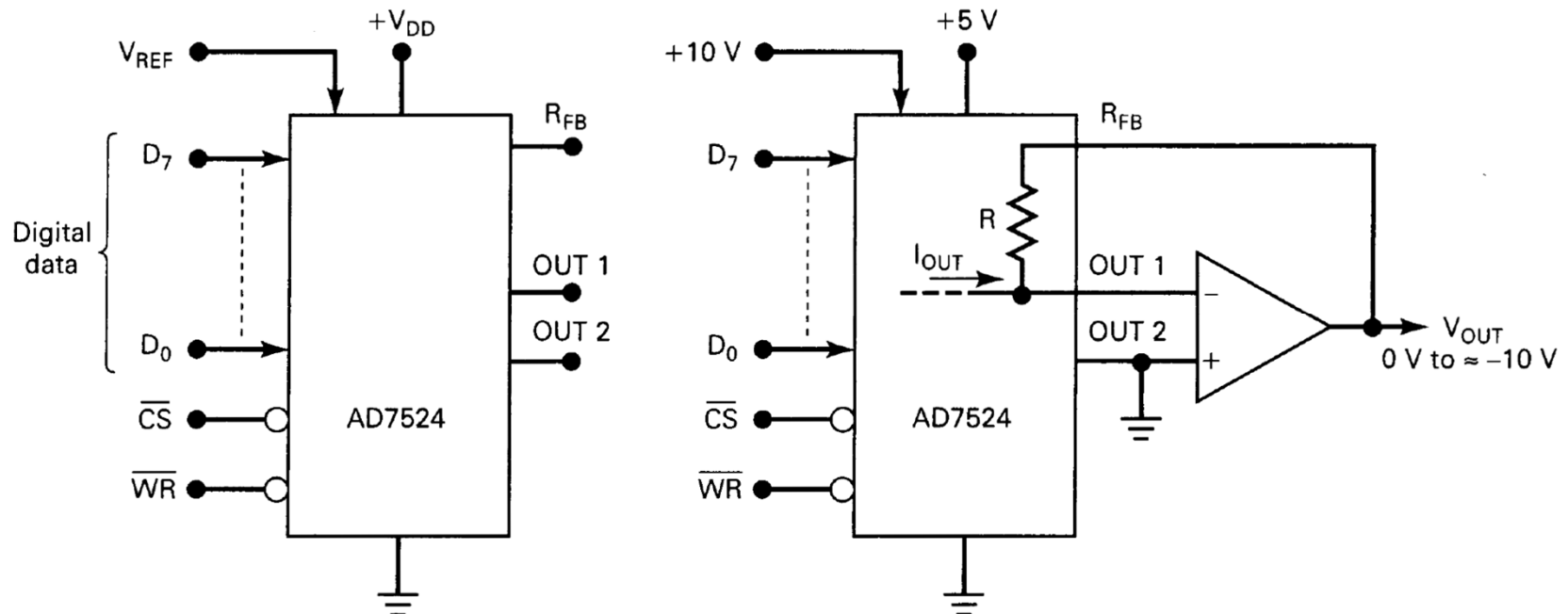
- Resolution
  - Depend on the number of bits
- Accuracy
  - Full-scale error: the maximum deviation of the DAC's output from its expected (ideal) value (% F.S.)
  - Linearity error: the maximum deviation in step size from the ideal step size (% F.S.)
- Offset Error
  - Very small output voltage when the binary input is all 0s. It can be negative or positive
  - Offset error will be added to the expected DAC output for all input cases

# DAC Specifications (2)

- Setting Time
  - Specify the operating speed of DAC
  - The time required for the DAC output to go from zero to full scale as the binary input is changed from all 0s to all 1s
  - Measured as the time for the DAC output to settle within  $\pm 1/2$  step size (resolution) of its final value
- Monotonicity
  - DAC is monotonic if its output increases as the binary input is incremented from one value the next.

# An Integrated-Circuit DAC

- AD7524: CMOS IC
  - 8-bit DAC that uses an R/2R ladder network
  - When Chip Select ( $\overline{CS}$ ) and WRITE ( $\overline{WR}$ ) signals are LOW, the digital data inputs  $D_7$ - $D_0$  produce the analog output current OUT1 (OUT2 is normally grounded)



# DAC Application

- Control
- Automatic Testing
- Signal Reconstruction
- A/D Conversion
- Serial DACs

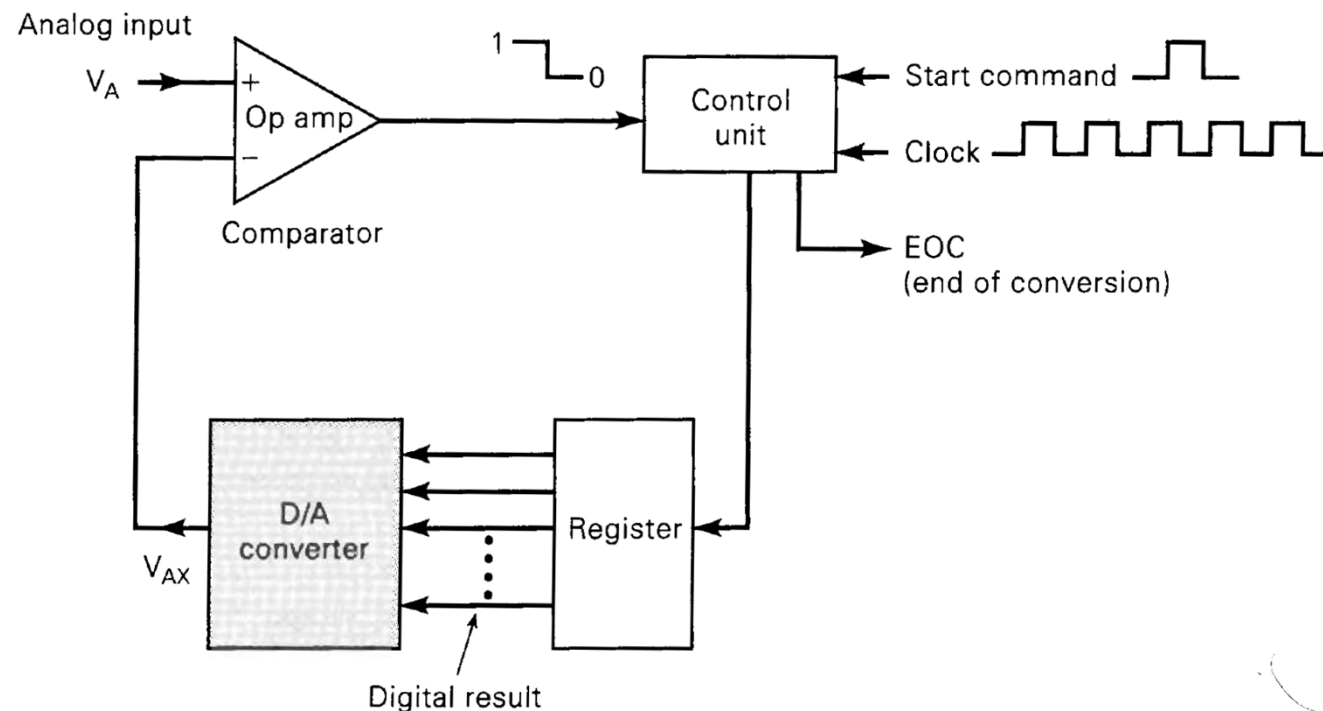
# Analog-to-Digital Conversion

- **Analog-to-Digital converter** (ADC) takes an analog input voltage and after a certain amount of time produces a digital output code that represents the analog input
- More complex
- Time-consuming



# Analog-to-Digital Conversion

- Several types of ADCs utilize a DAC as part of their circuitry
  - The timing for the operation is provided by the input clock signal
  - START COMMAND: initiate the conversion process



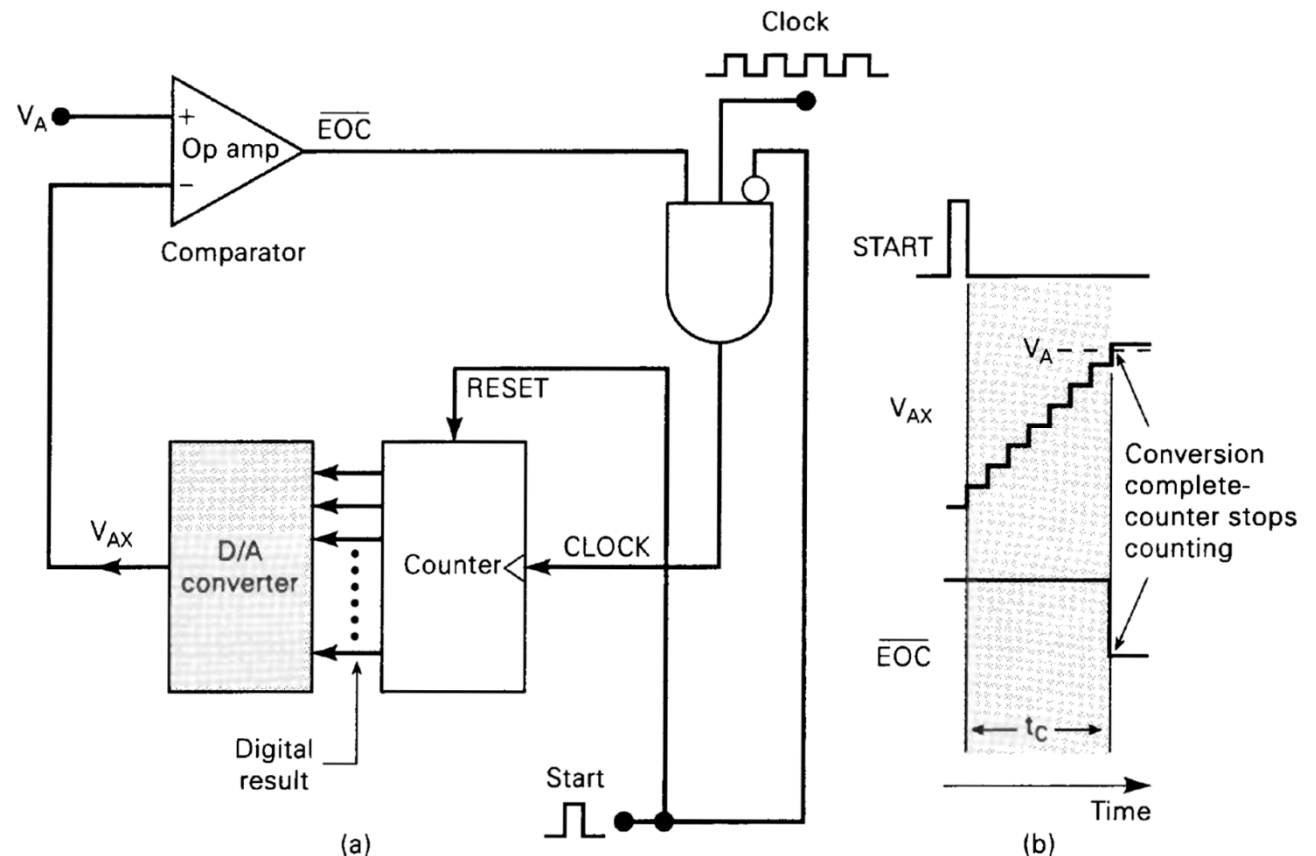
# Basic Operation of ADCs

- The START COMMAND pulse initiates the operation
- Control unit continually modifies the binary number that is stored in the register
- The binary number is converted to an analog voltage by the DAC ( $V_{AX}$ )
- The comparator compares  $V_{AX}$  with the analog input  $V_A$ 
  - If  $V_{AX} < V_A$ : the comparator output stays HIGH
  - If  $V_{AX} \geq V_A + V_T$  (**threshold voltage**): the comparator output goes LOW  $\rightarrow$  stop the process
    - $V_{AX}$  is a close approximation to  $V_A$
- Activate the end-of-conversion signal ( $\overline{\text{EOC}}$ ) when the conversion is complete

# Digital-Ramp ADC

- Simplest versions of the general ADC
- Use a binary counter as the register and allow clock to increment the counter one step at a time until

$$V_{AX} \geq V_A + V_T$$



# Digital-Ramp ADC – Example (1)

- ADC with the following values
    - Clock frequency = 1 MHz
    - $V_T = 0.1 \text{ (mV)} = 0.0001 \text{ (V)}$
    - DAC has F.S. output = 10.23 V and a 10-bit input
1.  $V_A = 3.728 \text{ V} \rightarrow \text{Digital value} = ?$
  2. Conversion time = ?
  3. The resolution = ?

## Digital-Ramp ADC – Example (2)

- DAC has 10-bit input and a 10.23-V F.S. output
  - Number of possible steps =  $2^{10} - 1 = 1023$
  - **Step size** =  $10.23 / 1023 = 10 \text{ mV}$
- $V_{AX}$  must reach  $V_A + V_T = 3.7281 \text{ (V)}$  or more before the comparator goes LOW
  - Number of steps
$$3.7281 \text{ V} / 10 \text{ mV} = 372.81 \approx 373$$
  - **Binary equivalent** = 0101110101
- The conversion requires 373 clock pulses
  - **Conversion time** =  $373 \times (1 / 1 \text{ MHz}) = 373 \mu\text{s}$
- Resolution = step size = 10 mV (0.1% F.S.)

# A/D Resolution and Accuracy

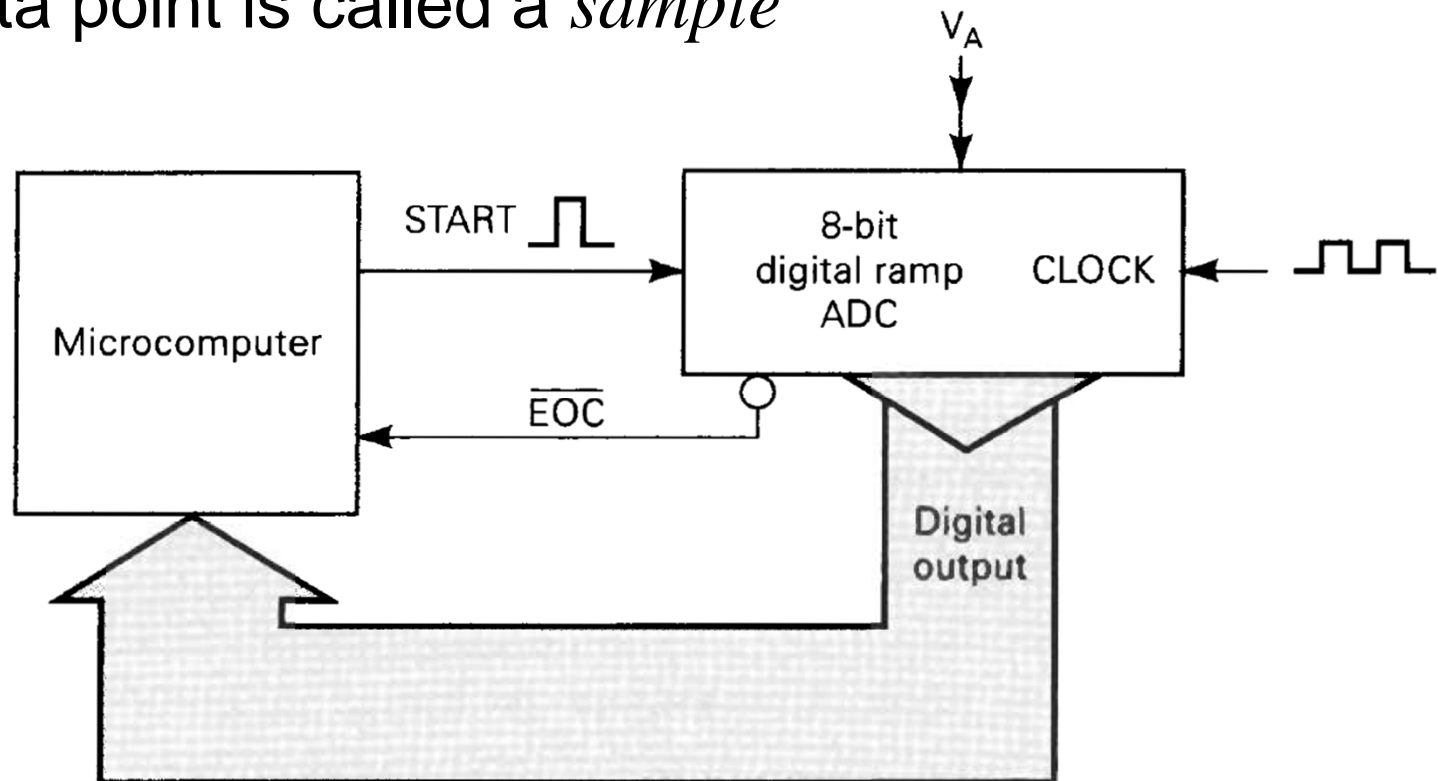
- An *unavoidable source of error* in the digital-ramp method: *step size* (resolution) of internal DAC is the smallest unit of measure
  - Reduce the potential error by making the step size smaller
  - **Quantization error**: a difference between the actual (analog) quantity and the digital value assigned to it
- Accuracy
  - Depend on the accuracy of the circuit components (comparator, resistor, reference supplies, v.v...)
  - This error is *in addition* to the quantization error due to resolution

# Conversion Time

- Conversion time ( $t_C$ ) is the time interval between the end of the START pulse and the activation of the EOC output
  - Maximum conversion time:  $V_A$  is just below full scale
$$t_C(\text{max}) = (2^N - 1) \text{ clock cycles}$$
  - Average conversion time: half of the maximum conversion time
$$t_C(\text{avg}) = t_C(\text{max}) / 2 = 2^{N-1} \text{ clock cycles}$$
  - Conversion time doubles for each bit that is added to the counter
  - Improve resolution  $\rightarrow$  longer  $t_C$
  - Unsuitable for high-speed A/D conversions

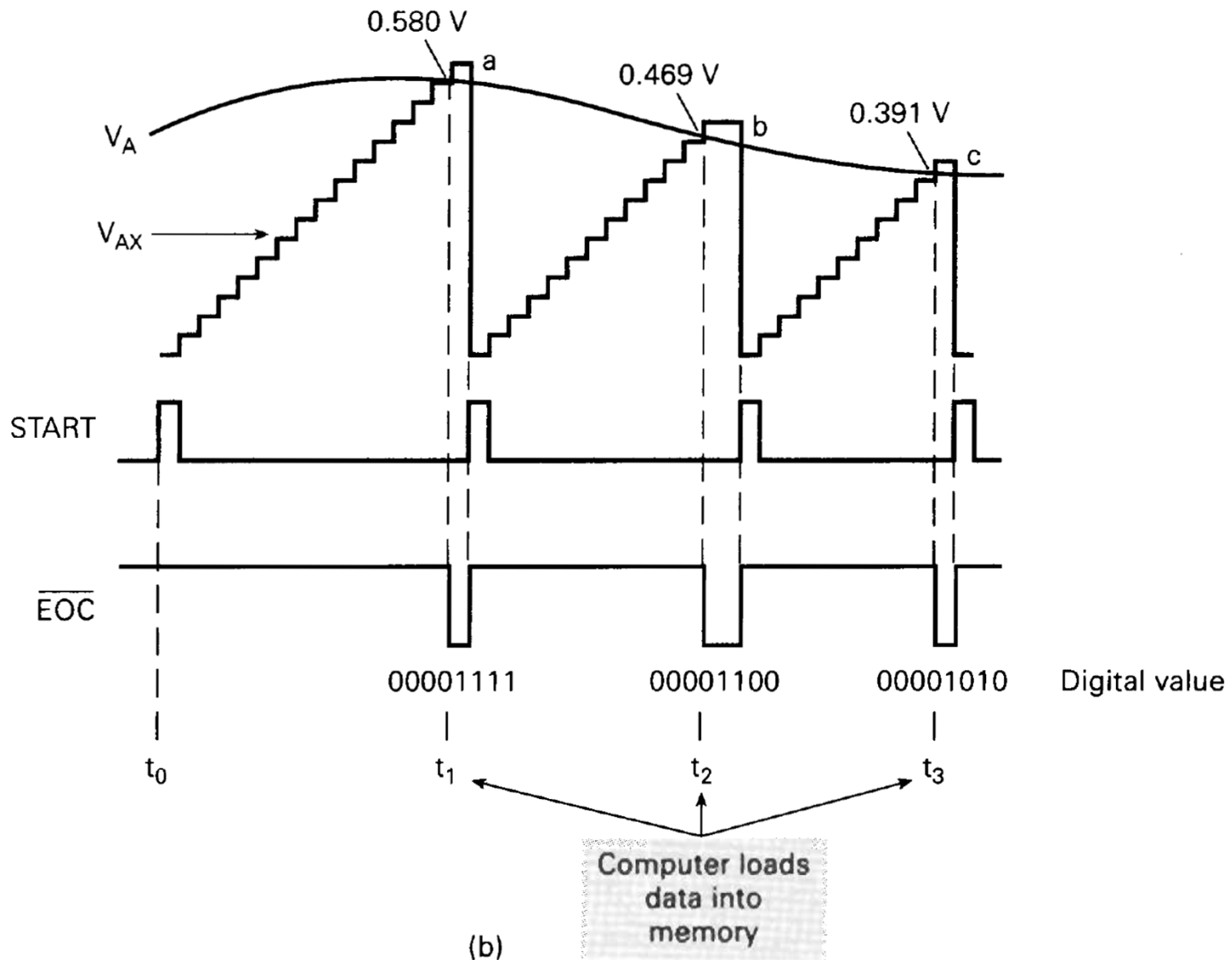
# Data Acquisition

- *Data acquisition*: The process by which the computer acquires the digitized analog data
- *Sampling*: acquiring a single data point's value
  - Data point is called a *sample*

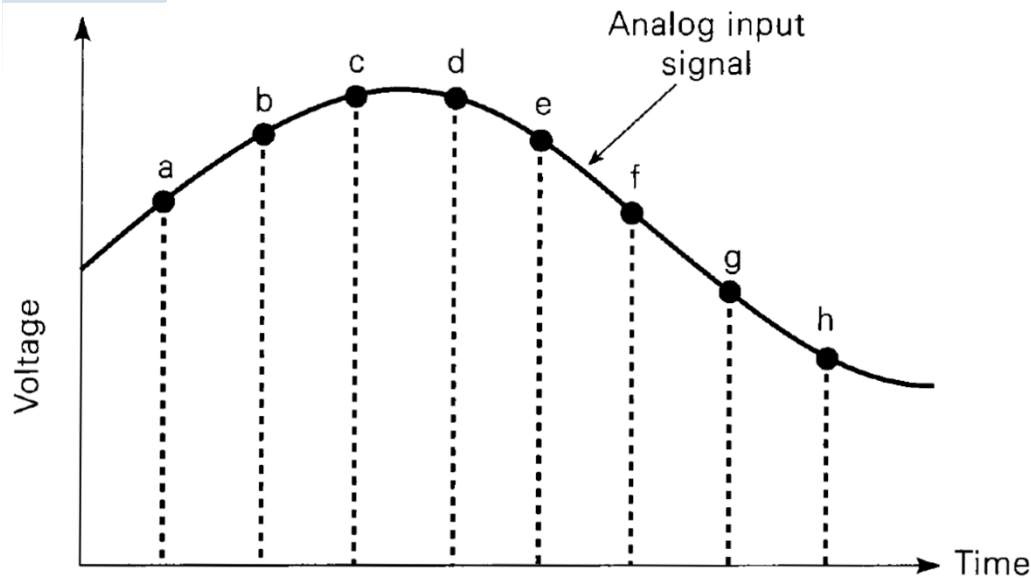




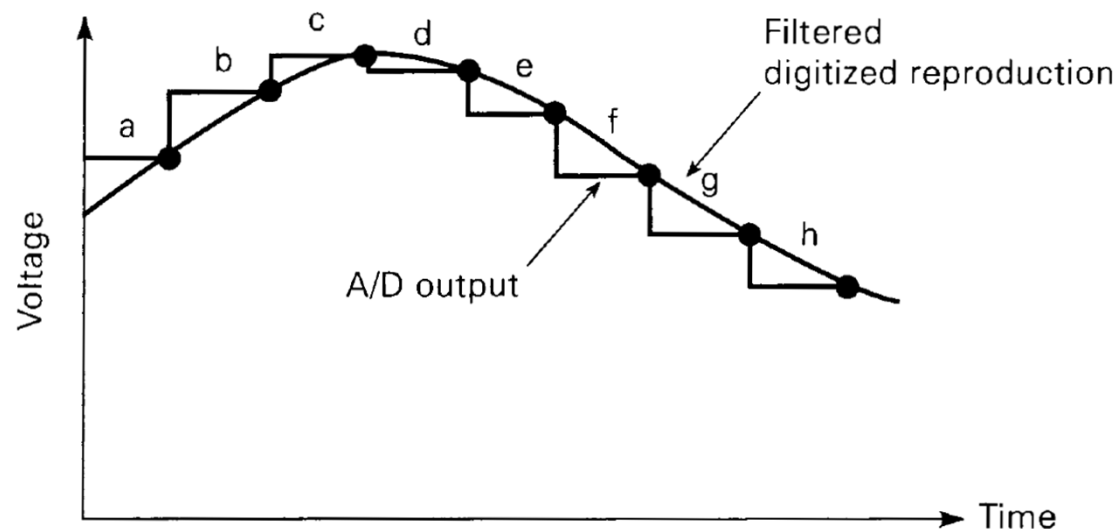
# Data Acquisition



# Reconstructing a Digitized Signal



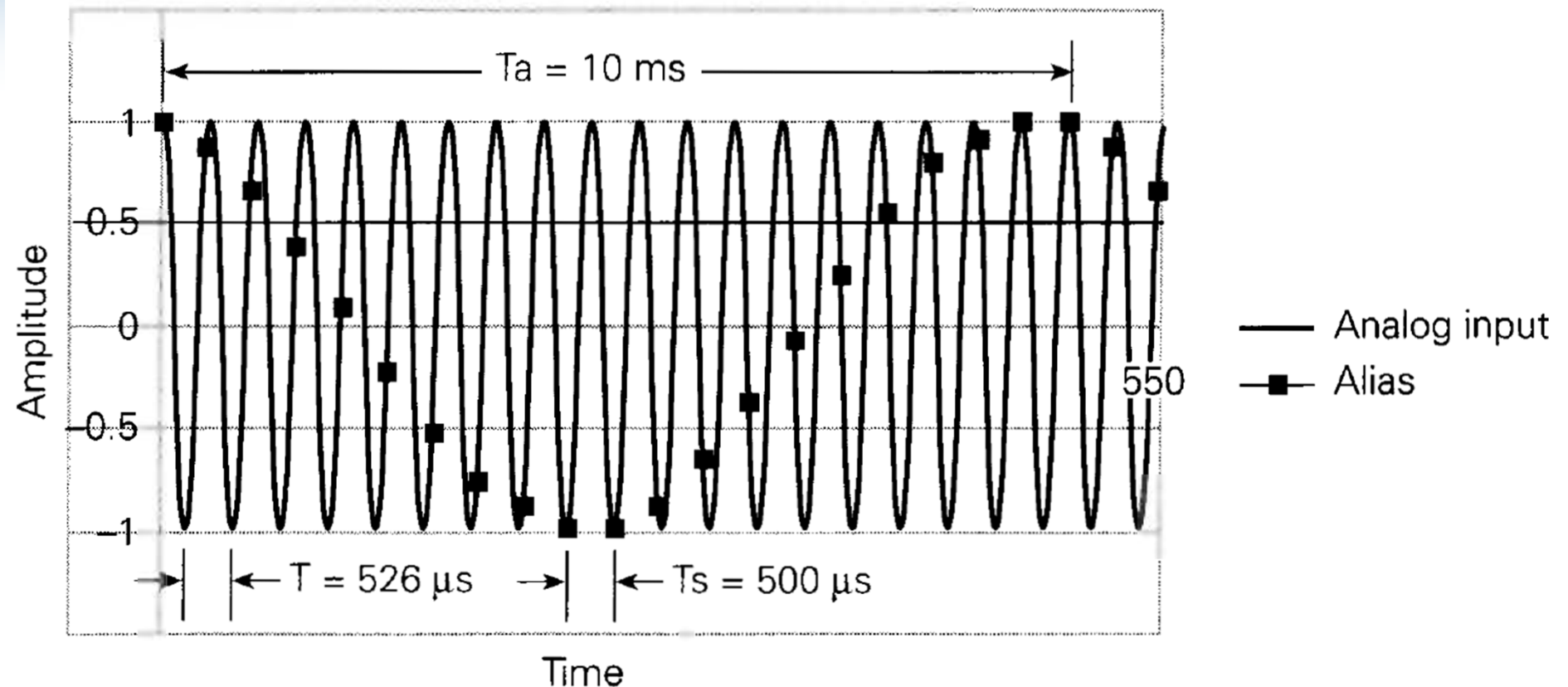
Point	Actual Voltage (V)	Digital Equivalent
<i>a</i>	1.22	01111010
<i>b</i>	1.47	10010011
<i>c</i>	1.74	10101110
<i>d</i>	1.70	10101010
<i>e</i>	1.35	10000111
<i>f</i>	1.12	01110000
<i>g</i>	0.91	01011011
<i>h</i>	0.82	01010010



# Aliasing

- Nyquist sampling theorem: **Sampling frequency** ( $F_s$ ) must be at a rate greater than two times the highest-frequency component in the incoming signal
- A signal **alias** is produced by sampling the signal at a rate less than the minimum rate identified by Nyquist
- **Under-sampling** ( $F_s < 2F_{in \text{ max}}$ )
  - Digital system has no idea that there was actually a higher frequency at the input

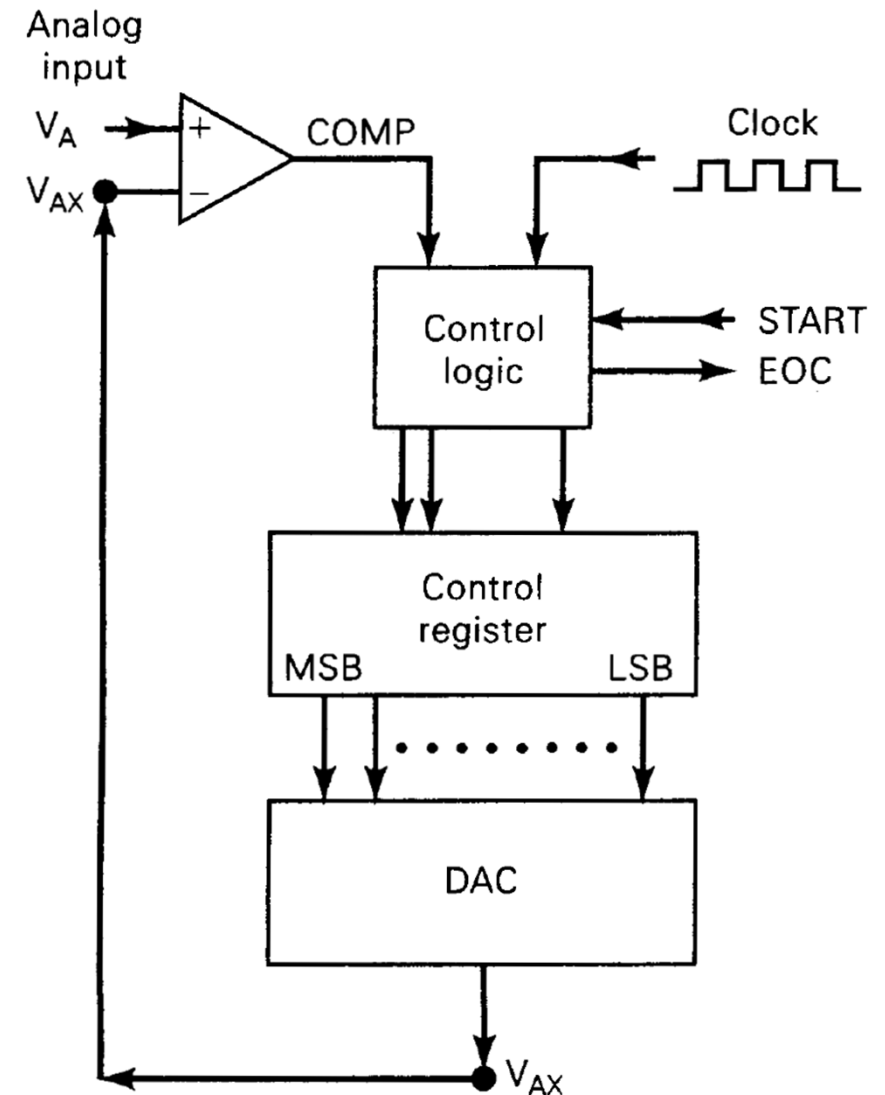
# Aliasing

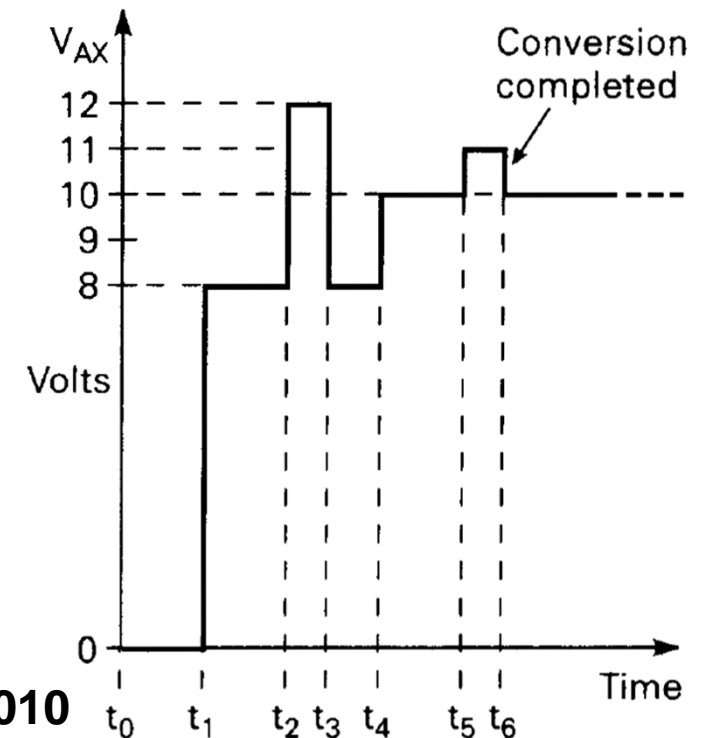
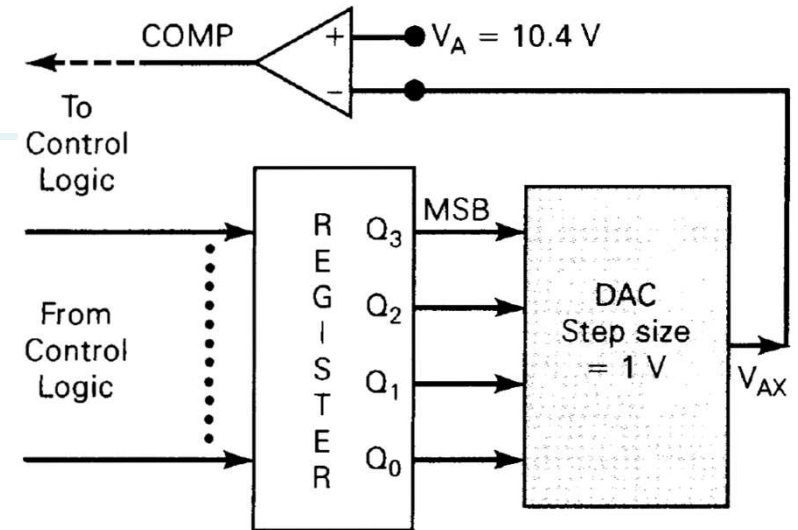
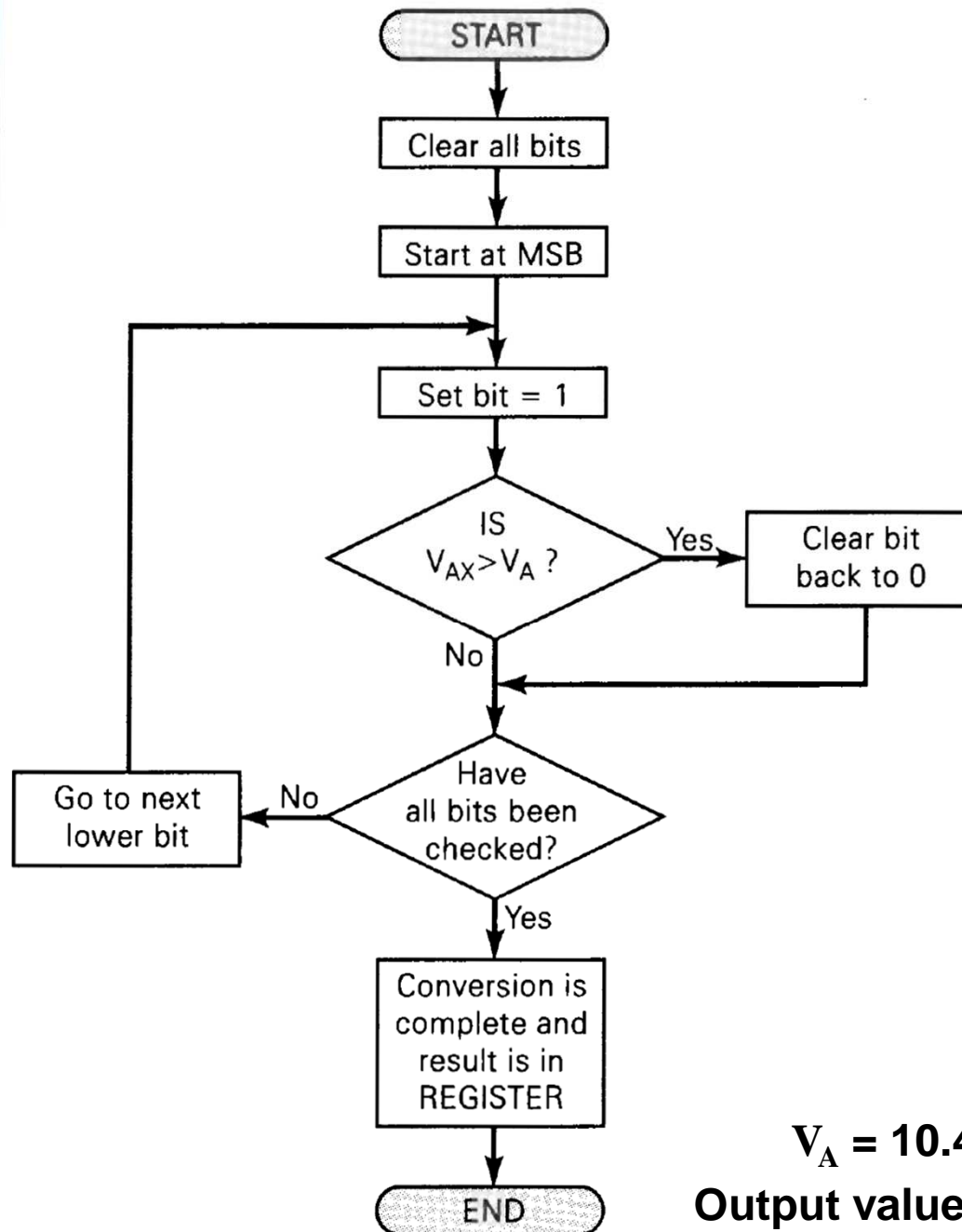


- Analog signal:  $F = 1.9 \text{ kHz}$
- Sampling frequency:  $F_s = 2 \text{ kHz}$
- Alias signal:  $F = 100 \text{ Hz}$

# Successive-Approximation ADC (SAC)

- More complex circuitry than the digital-ramp ADC
- Use register to provide the input to the DAC block
- The digital output is equivalent to a voltage that is less than the analog input  $V_A$





$V_A = 10.4\text{ V}$   
Output value = 1010

# SAC – Conversion time

- Much shorter conversion time
  - Fixed value conversion time
  - Not dependent on the value of the analog input
- Total conversion time for an N-bit SAC:  $N$  clock cycles

$$t_C \text{ for SAC} = N \times 1 \text{ clock cycle}$$

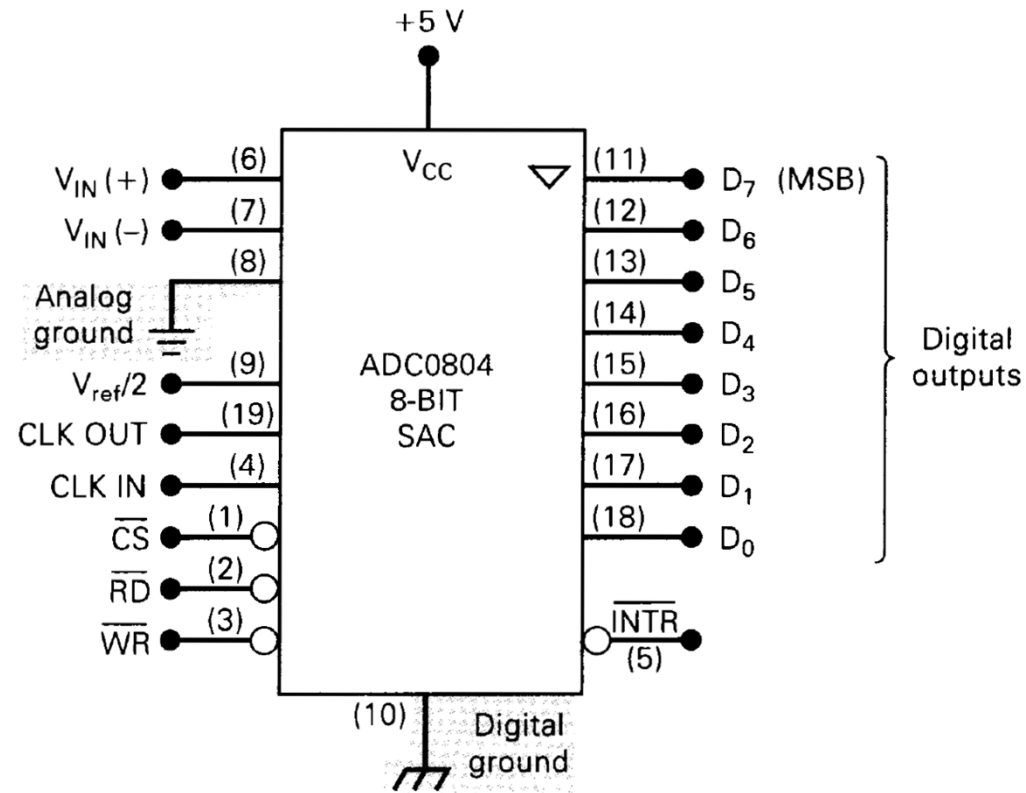
- Example: two ADCs utilize a 500-kHz clock frequency
  - 10-bit digital-ramp ADC:  $t_C = (2^{10} - 1) \times 2 \mu\text{s} = 2046 \mu\text{s}$
  - 10-bit SAC:  $t_C = 10 \times 2 \mu\text{s} = 20 \mu\text{s}$
- In *data acquisition*: permit more data values to be acquired in a given time interval

# The ADC0804

- 20-pin CMOS IC
- Using the successive-approximation method
- Characteristics
  - 2 analog inputs  $V_{IN}(+)$  and  $V_{IN}(-)$  to allow **differential inputs**
  - 8-bit digital output, **tristate** buffered → connected in a data bus arrangement
  - An internal clock generator circuit,  $f = 1/(1.1RC)$
  - $f = 606\text{-kHz}$  ( $R = 10\text{ k}\Omega$ ,  $C = 150\text{ pF}$ ) → conversion time  $100\text{ }\mu\text{s}$
  - Separate ground connections for digital and analog voltages



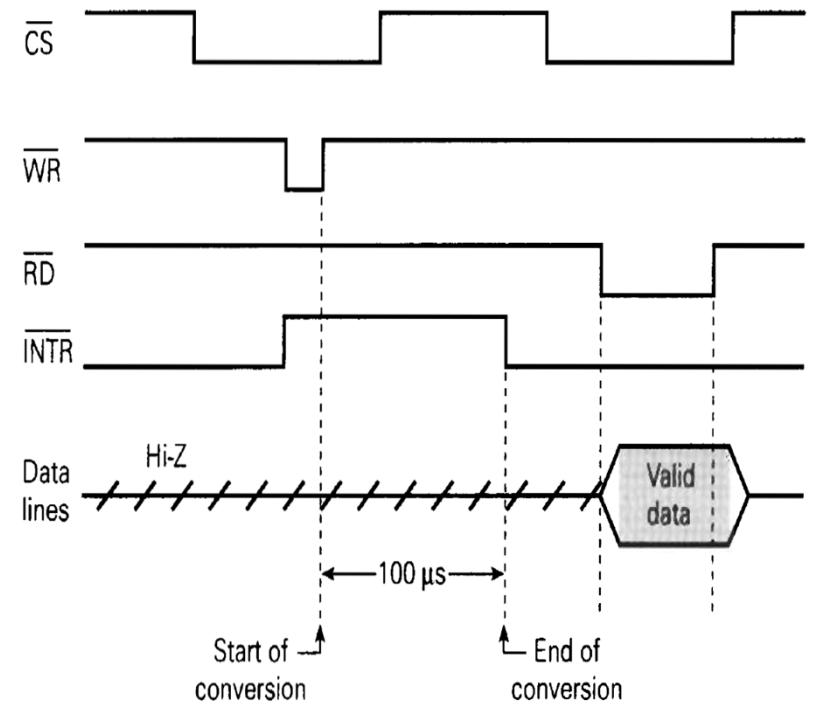
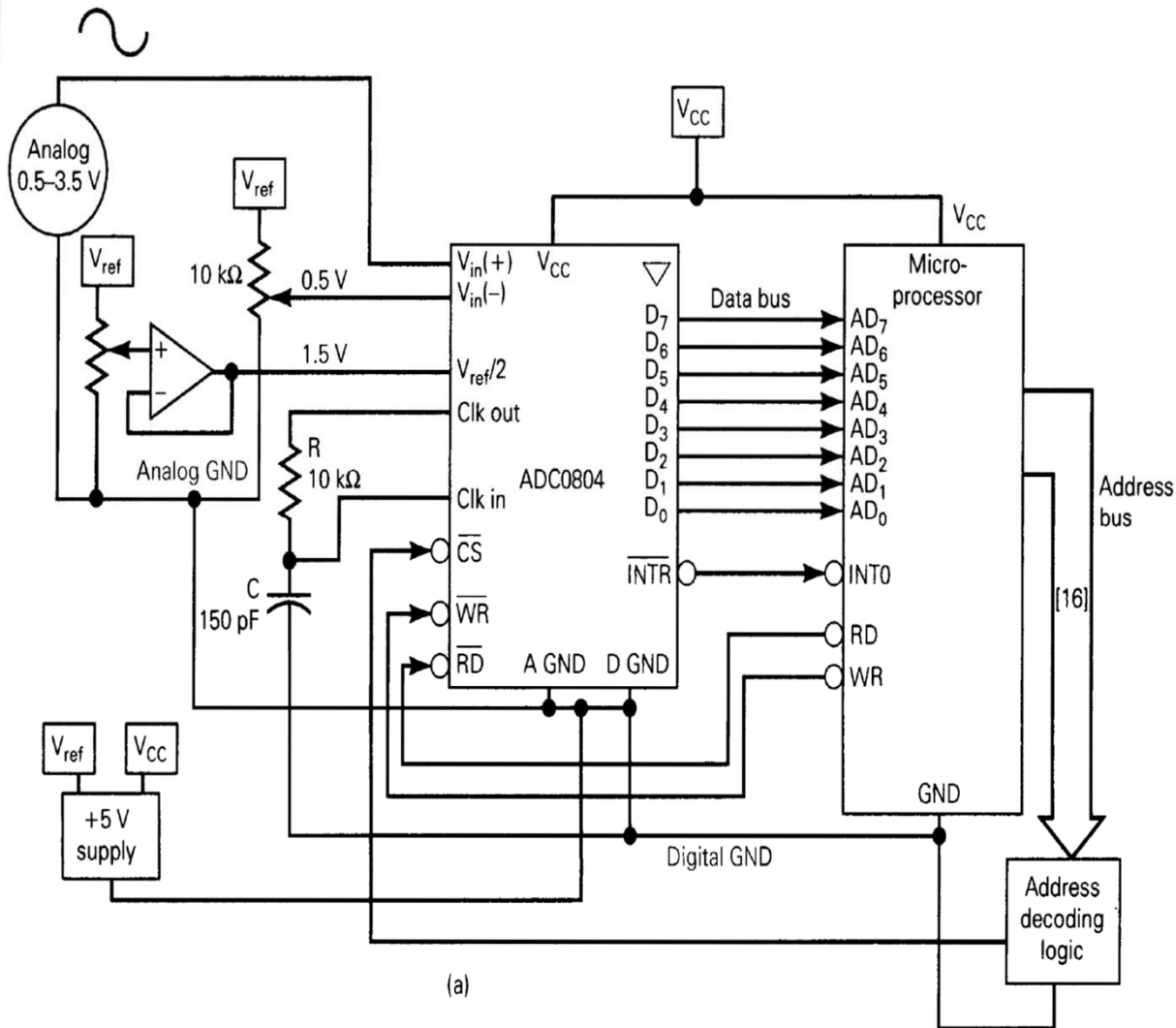
# The ADC0804



$V_{ref}/2$	Analog Input Range (V)	Resolution (mV)
Open	0–5	19.6
2.25	0–4.5	17.6
2.0	0–4	15.7
1.5	0–3	11.8

# dce 2013

## The ADC0804

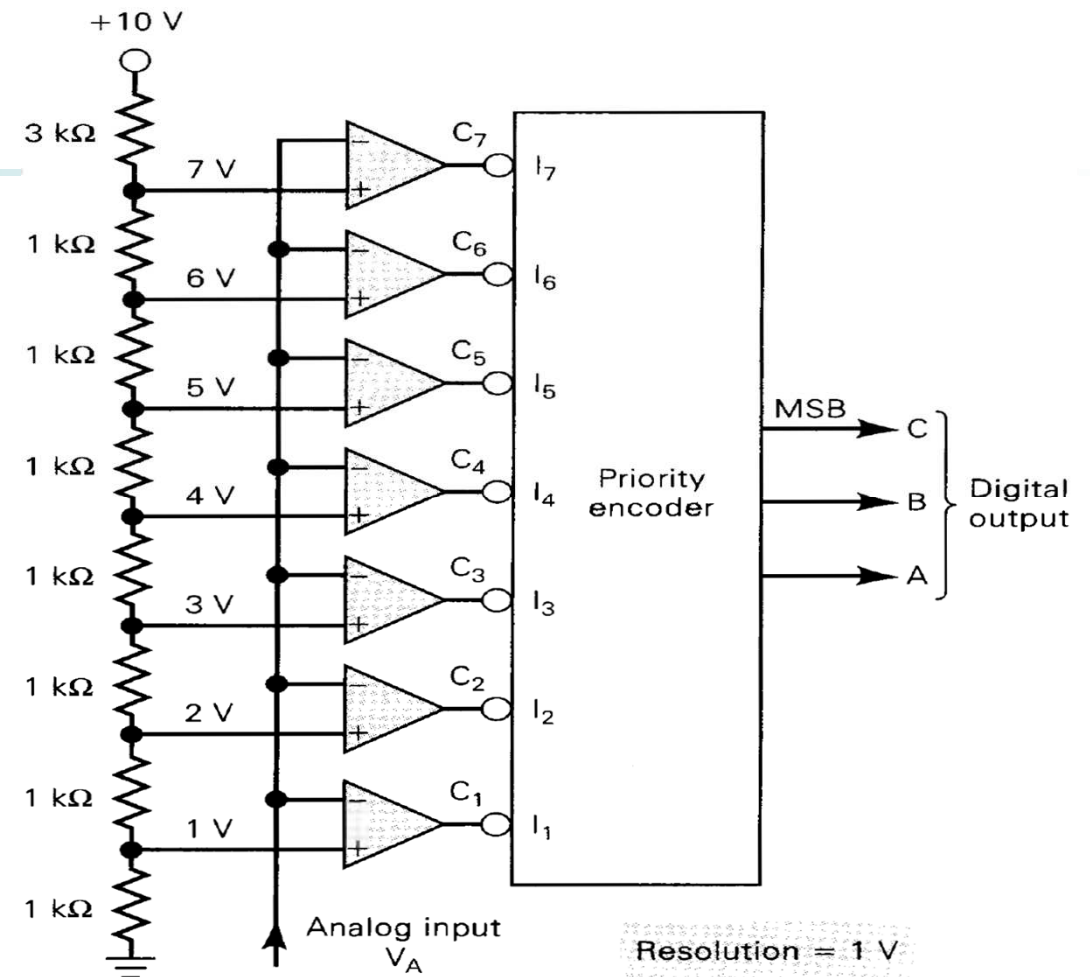


# Flash ADCs

- The highest-speed ADC
- Require much more circuitry, the large number of comparator limits the size of flash converters
- N-bit flash converter require  $2^N - 1$  comparators,  $2^N$  resistors, and the necessary encoder logic
- Conversion time: depend only on the propagation delays of the comparators and encoder logic

# Flash ADCs

- Use the voltage-divider resistors
- Priority encoder



Analog in $V_A$	Comparator outputs							Digital outputs		
	$C_1$	$C_2$	$C_3$	$C_4$	$C_5$	$C_6$	$C_7$	C	B	A
0-1 V	1	1	1	1	1	1	1	0	0	0
1-2 V	0	1	1	1	1	1	1	0	0	1
2-3 V	0	0	1	1	1	1	1	0	1	0
3-4 V	0	0	0	1	1	1	1	0	1	1
4-5 V	0	0	0	0	1	1	1	1	0	0
5-6 V	0	0	0	0	0	1	1	1	0	1
6-7 V	0	0	0	0	0	0	1	1	1	0
> 7 V	0	0	0	0	0	0	0	1	1	1

# Other A/D Conversion Methods (1)

- **Up/Down Digital-Ramp ADC (Tracking ADC)**
  - Use an up/down counter to reduce the wasted time
    - $V_{AX} > V_A \rightarrow$  Count down
    - $V_{AX} < V_A \rightarrow$  Count up
  - New conversion: the counter is *not reset to 0* but begin from the last value
- **Dual-Slop Integrating ADC**
  - The slowest conversion times
  - Basic operation: *linear* charging and discharging of a capacitor using constant currents
  - Use a counter to hold a count proportional to the initial capacitor voltage at the end of the discharge interval

# Other A/D Conversion Methods (1)

- **Voltage-to-Frequency ADC**

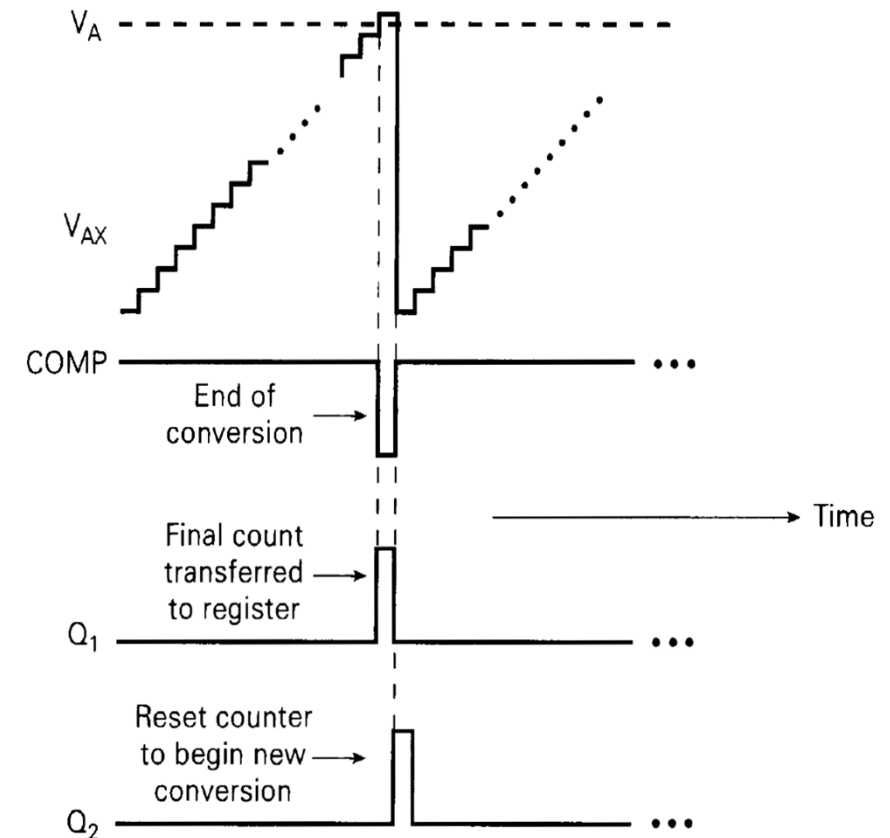
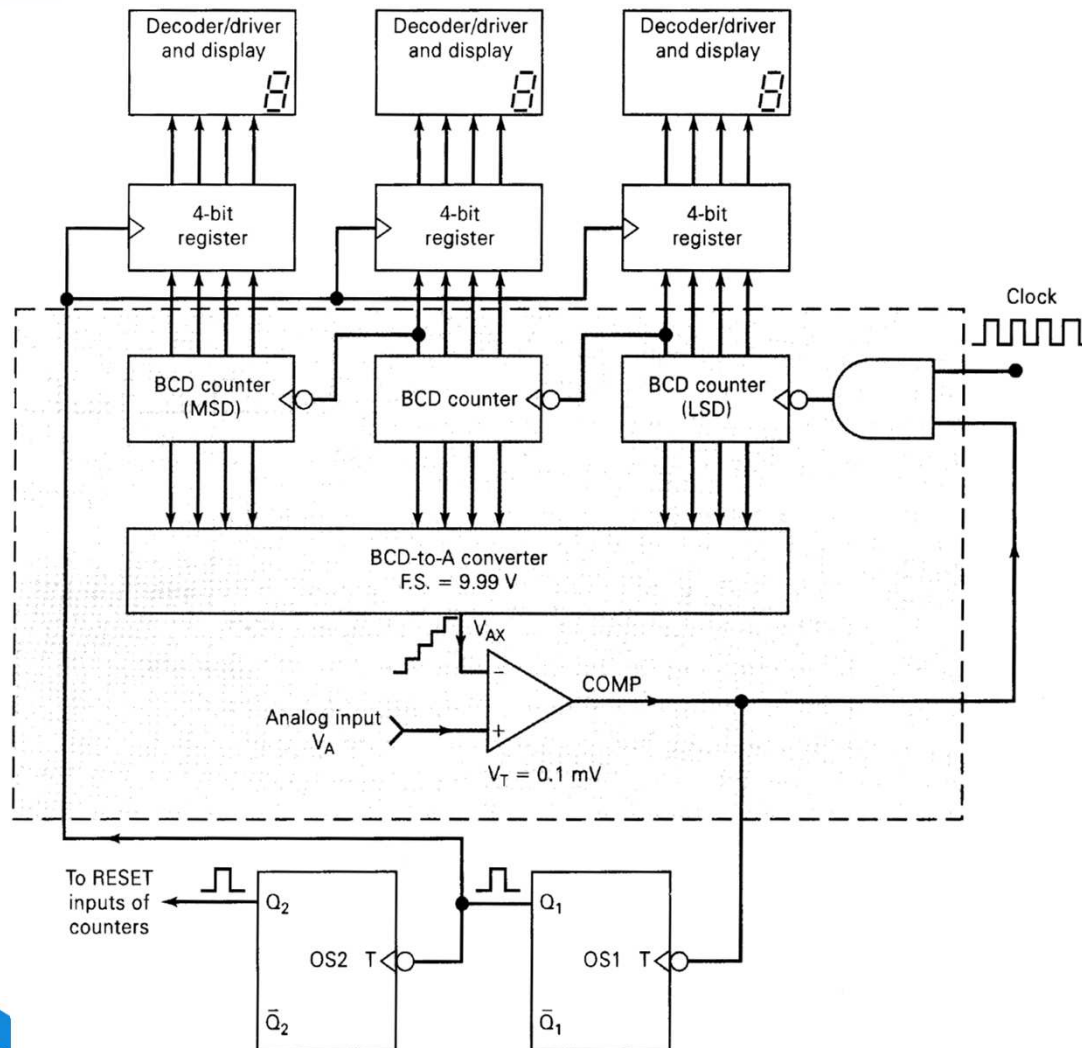
- Not use a DAC
- Use a *linear voltage-controlled oscillator (VCO)*: produce an output frequency proportional to the input voltage
- Output frequency is fed to a counter to be counted for a fixed time interval → proportional to the value of the analog voltage

- **Sigma/Delta Modulation**

- Sample the analog information more often than the minimum sample rate ( $2F_{IN}$  max) (*oversampling*)
- Represent the analog voltage by varying the density of logic 1s in a single-bit stream of serial data

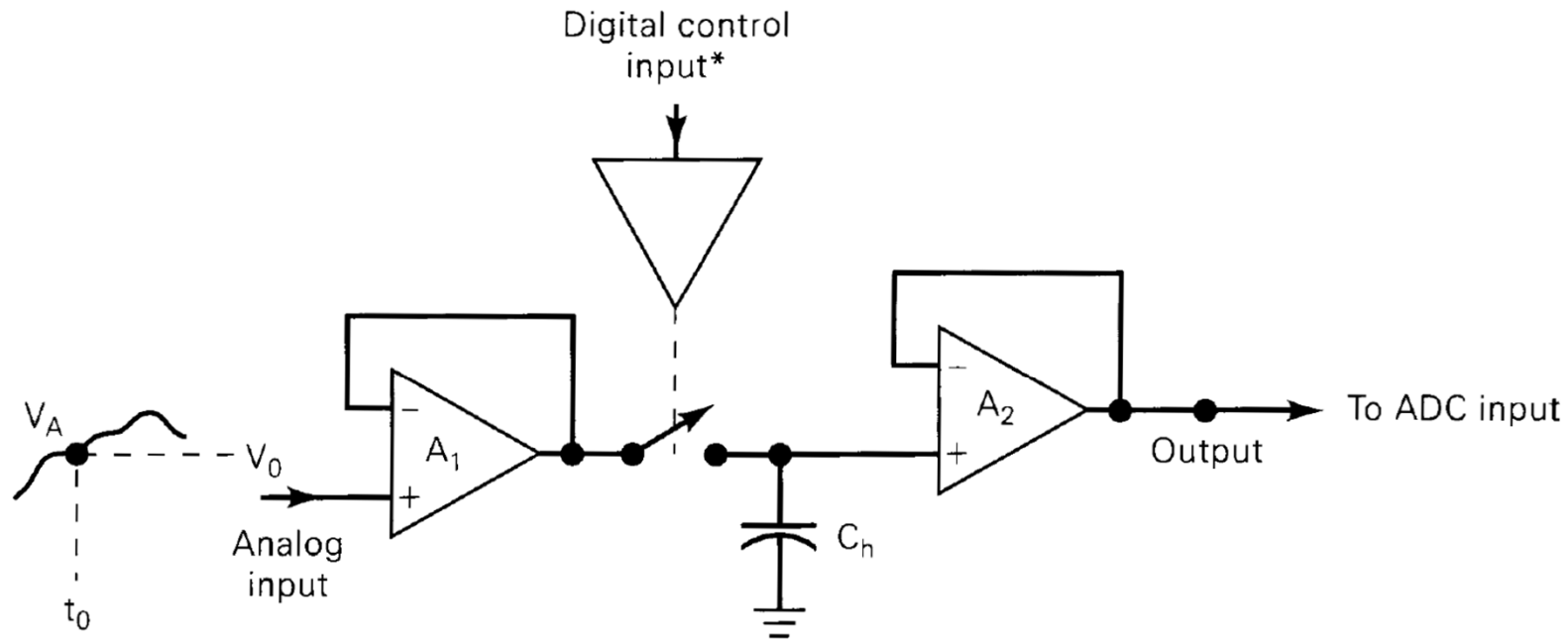
# Digital Voltmeter (DVM)

- DVM converts an analog voltage to its BCD-code



# Sample-And-Hold Circuits

- Hold the analog voltage constant while the A/D conversion is taking place
  - Sample mode:  $C_h$  is charged during **acquisition time**
  - Hold mode:  $C_h$  will hold the voltage

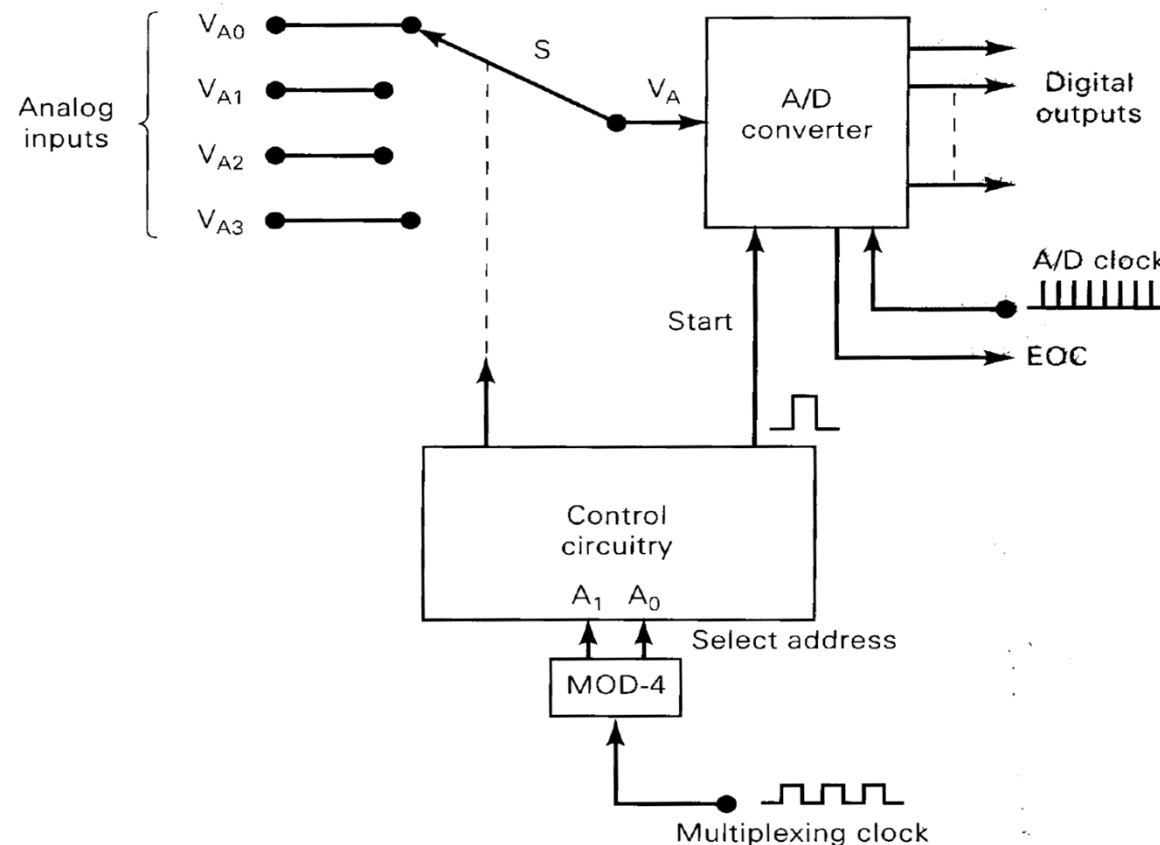


\*Control = 1 → switch closed → sample mode  
Control = 0 → switch open → hold mode

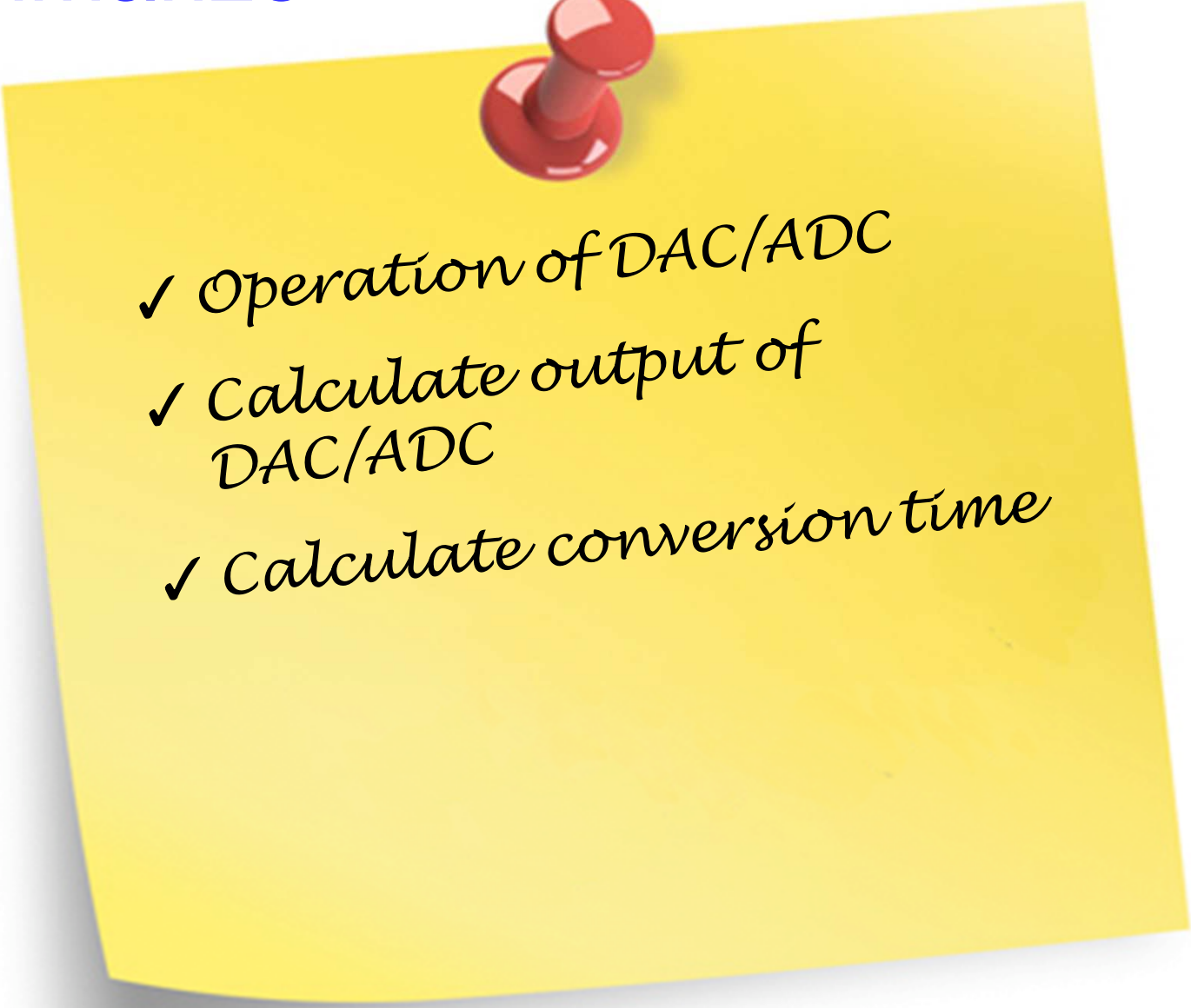


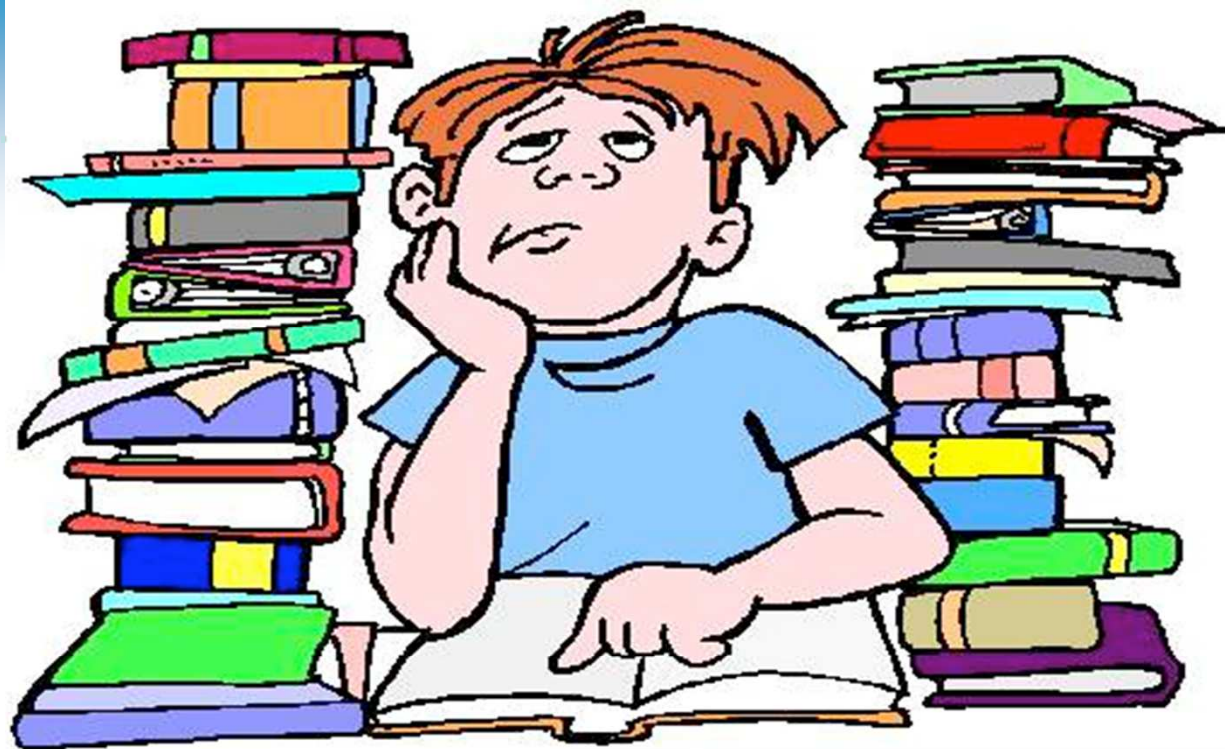
# Multiplexing

- Multiplexing technique allows a common ADC to be *time-shared* between several analog input sources



# Summarize

- 
- ✓ Operation of DAC/ADC
  - ✓ Calculate output of DAC/ADC
  - ✓ Calculate conversion time



# Reference

- Chapter 10, Digital System – Principles and Applications, Ronald J.Tocci, Neal S. Widmer